TE1 Block Diagram

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

VCC_CORE
+1.5V
+1.05V
+1.25V
+1.8VSUS
+1.8V
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

HDMI Page 21 — HDMI — Transmitter Sil1392 Page 21 — Azalia

CRT Page 20

LCD PANEL Page 19

LED PANEL Page 19 — LED Driver IC Page 19

SATA - HDD Page 22

IDE - ODD Page 22

Intel Merom (35W) Page 3,4

FSB(667/800MHZ)

CLOCK GENERATOR CK505 ICS9LPR363 Page 2

Azalia — VGA CONNECTOR (FOX) Page 18 — CRT, HDMI, LCD/LED

PCI-E 16X Lan

533/ 667 MHZ DDR II — DDRII-SODIMM1 DDRII-SODIMM2 Page 12,13

SDVO

CRT

LVDS

SATA

PATA

Crestline GM Page 5,7,8,9,10,11

DMI(x2/x4)

MINI CARD-3 U 9H_HD-DVD Page 25

MINI CARD-4 D ROBSON Page 25 (FTB)

PCI-Express

PCIE-2 — PCIE-4 — PCIE-6 — PCIE-3 — PCIE-1 — PCIE-5

MINI CARD-1 U&D 5.6H_WLAN Page 25

MINI CARD-2 U 6.75H_TV/ROBSON D 7.5H_HD-DVD Page 25

NEW CARD Page 27

Connector Page 26

LAN/RJ11/RJ45/USB/RF DAUGHTER BOARD

Marvell LAN 10/100/Giga 88E8040T/88E8072

Transformer

RJ45 — RJ11 — USB — RF

DAUGHTER BOARD

LED Board

Low Cost Board Page 26

MMB Board Page 26

Power Board Page 26

Touch Pad Board Page 26

DAUGHTER BOARD

LAN/B USB Page 26 (FTB) — USB-0

Camera Page 19 — USB-3

WLAN Page 25 — USB-5

Finger Printer Page 26 (FTB) — USB-1

Bluetooth Page 26 — USB-2

New Card Page 27 — USB-9

M/B USB 2 Page 27 — USB-7

Felica Page 26 (FTB) — USB-4

M/B USB Page 27 — USB-6

TV/ROBSON Page 25 — USB-8

USB 2.0

ICH8M Page 14,15,16,17

Azalia

PCI Bus

LPC

32.768KHz

PCMCIA Controller (CB 1410) Page 23 — PCMCIA

Card Reader/1394 (OZ129T) Page 24 — 5 IN 1 — 1394

WPCE775C Page 28

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD18	INTC#	CB1410

VR Page 30 — FAN Page 3 — Kill SW Page 27 — Key Board Page 26 — FLASH ROM Page 28 — CIR Page 28 — G-Sensor Page 22

HP Page 30 — Port-A — Port-B

MIC JACK Page 30

INT SPK Page 29 — SPK AMP Page 29

AUDIO CODEC (CX20561) Page 29

Port-C

FM TUNER & MDC Page 30 — Reserve FM Page 29

Reserve MIC Page 19

Reserve MIC Page 29

MDC Board — RJ11

BTO BOM OPTION

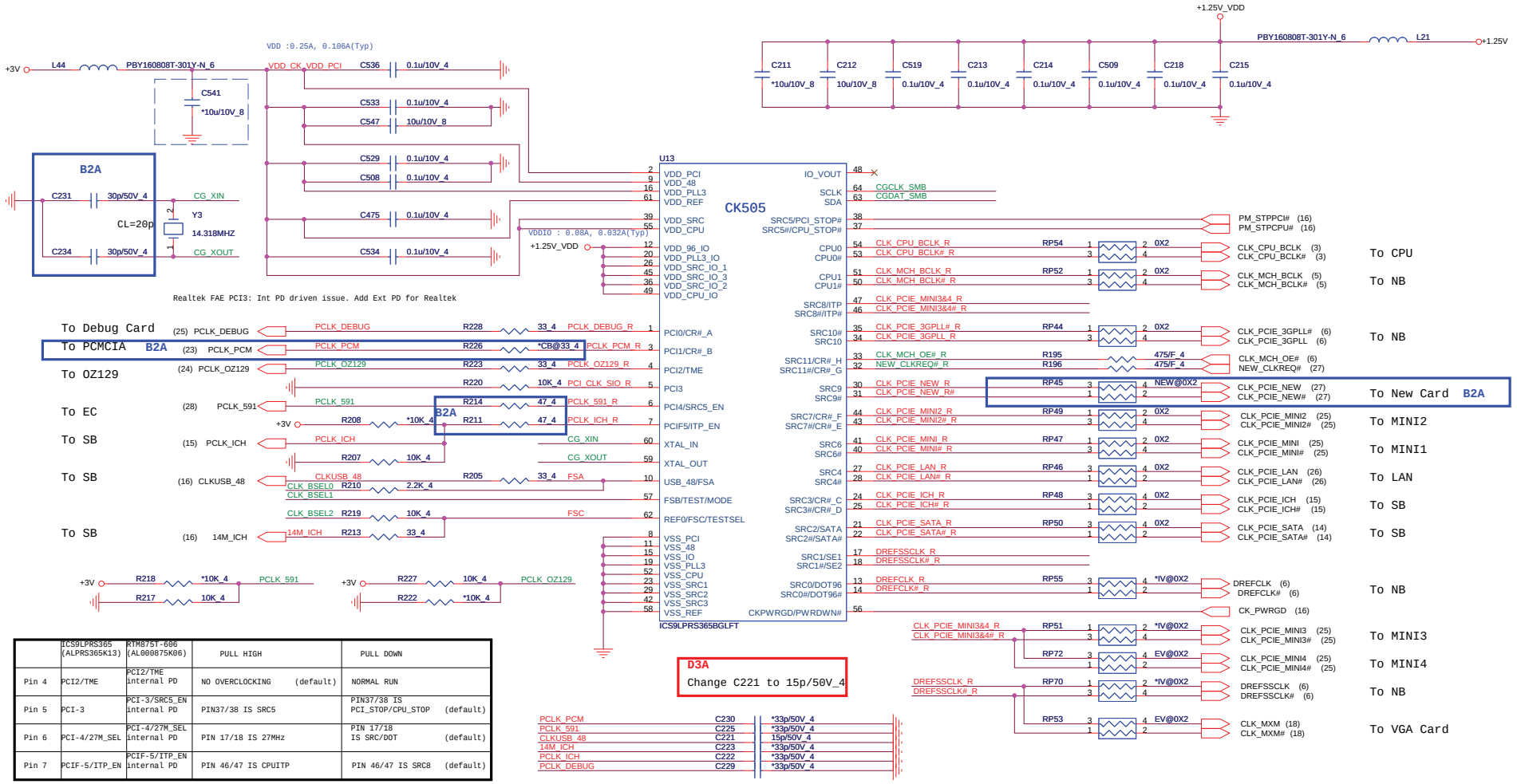
IV@ : UMA
EV@ : VGA/B
CB@ : CARD_BUS
GS@ : G-SENSOR
NEW@ : NEW CARD
LCD@ : LCD TYPE PANEL
LED@ : LED TYPE PANEL
CIR@ : CIR

Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	Block Diagram	1A

Date: Saturday, January 19, 2008 Sheet 1 of 41

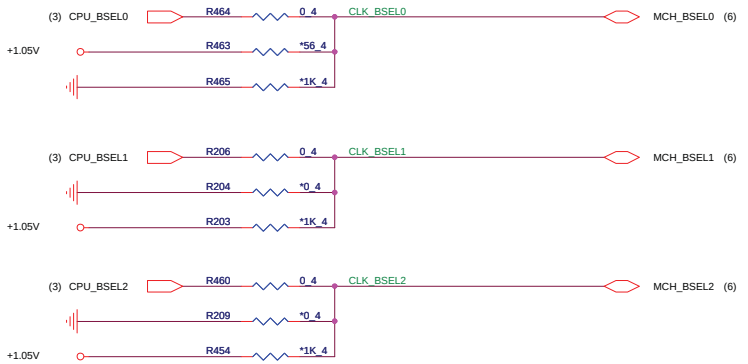
Clock Generator



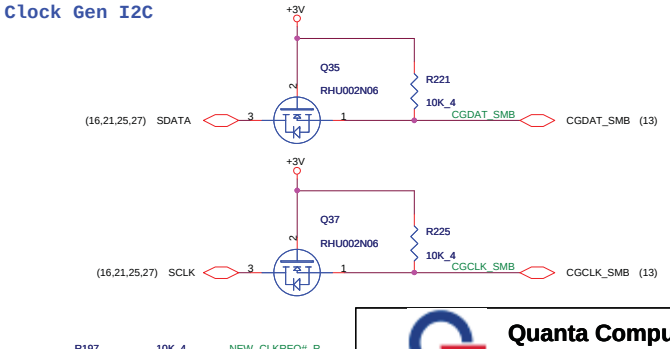
	ICS9LPRS365 (ALPRS365K13)	RTM875T-686 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

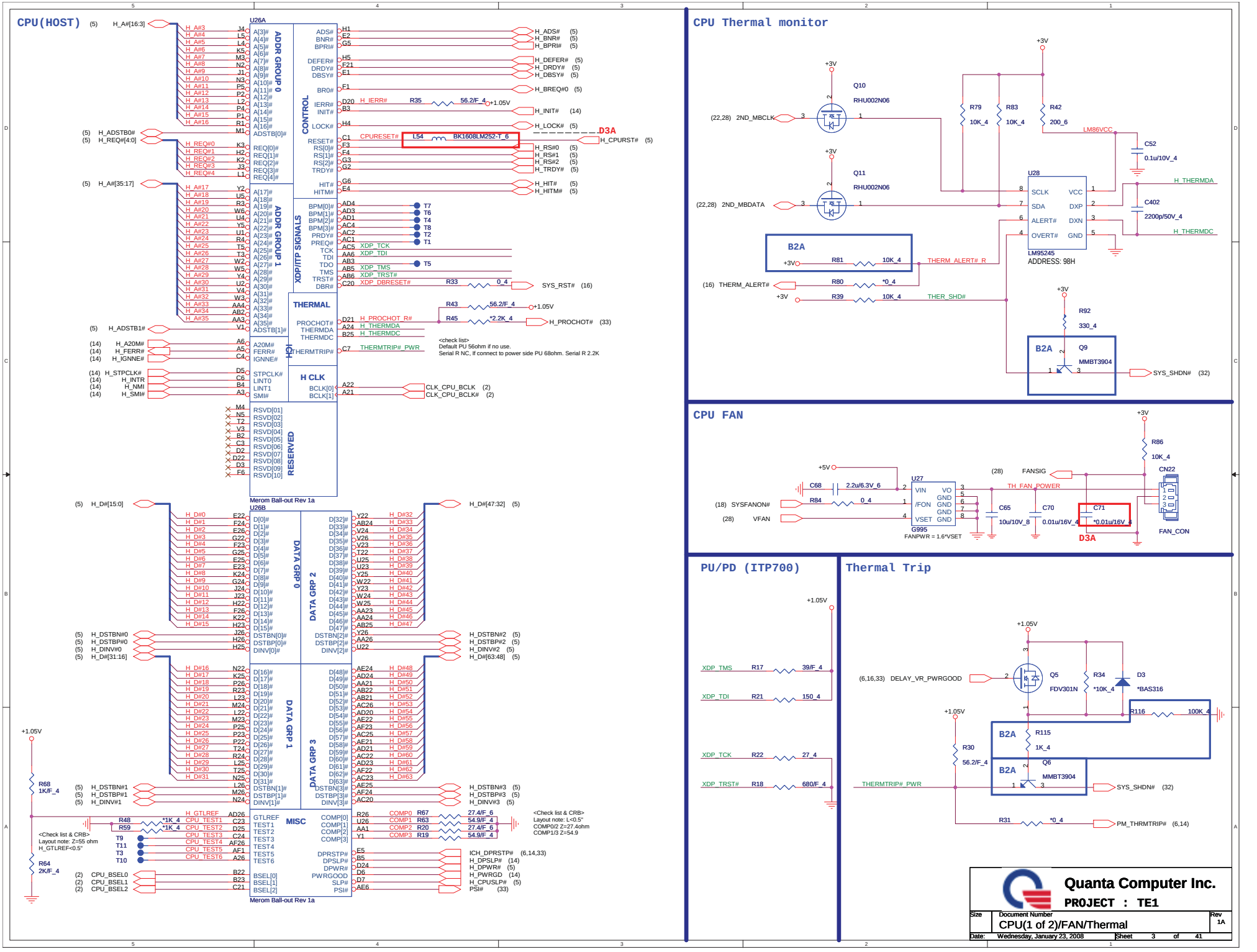


Clock Gen I2C

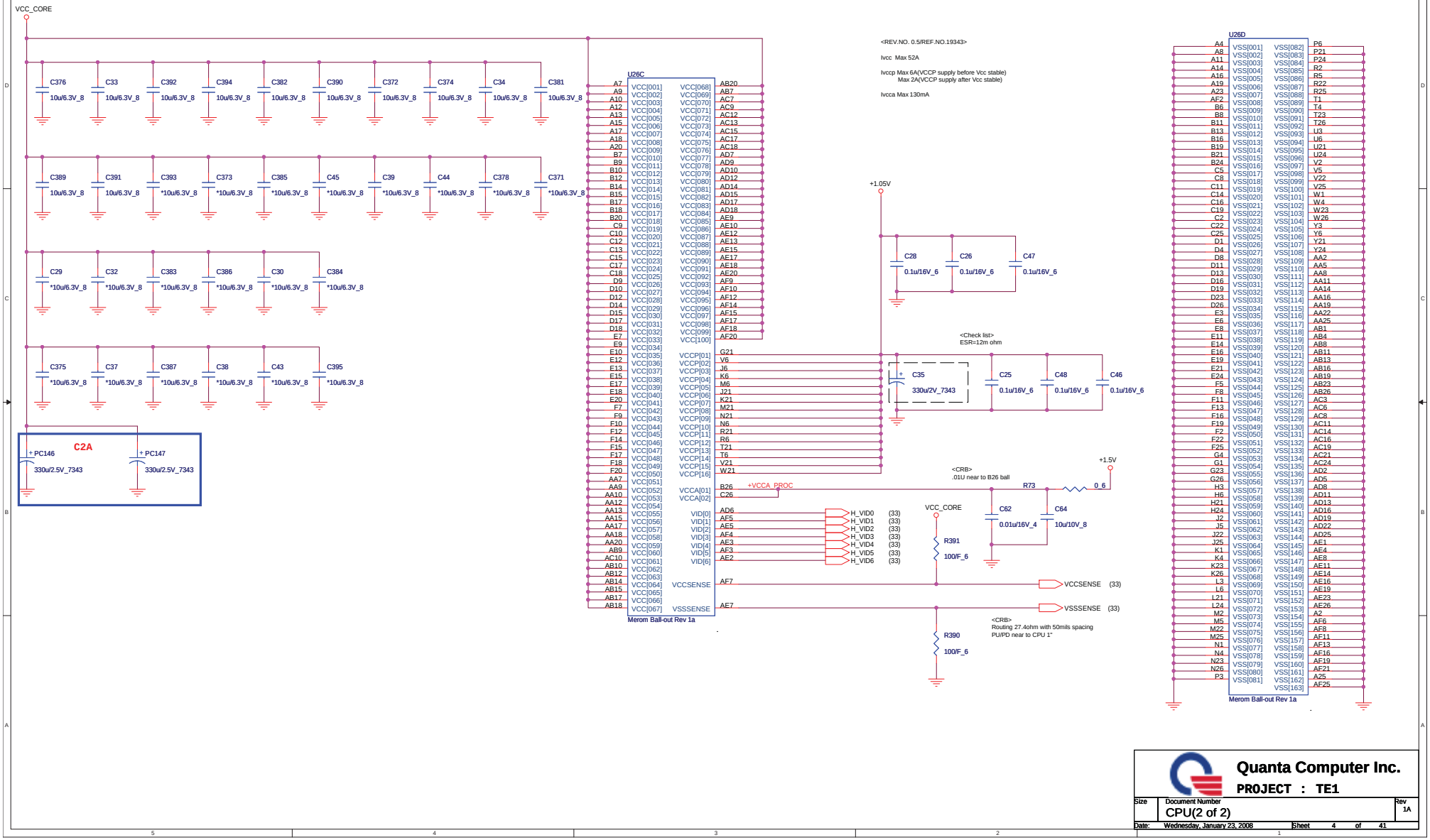


Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	CLK. GEN./ CK505	1A
Date: Wednesday, January 23, 2008	Sheet 2 of 41	

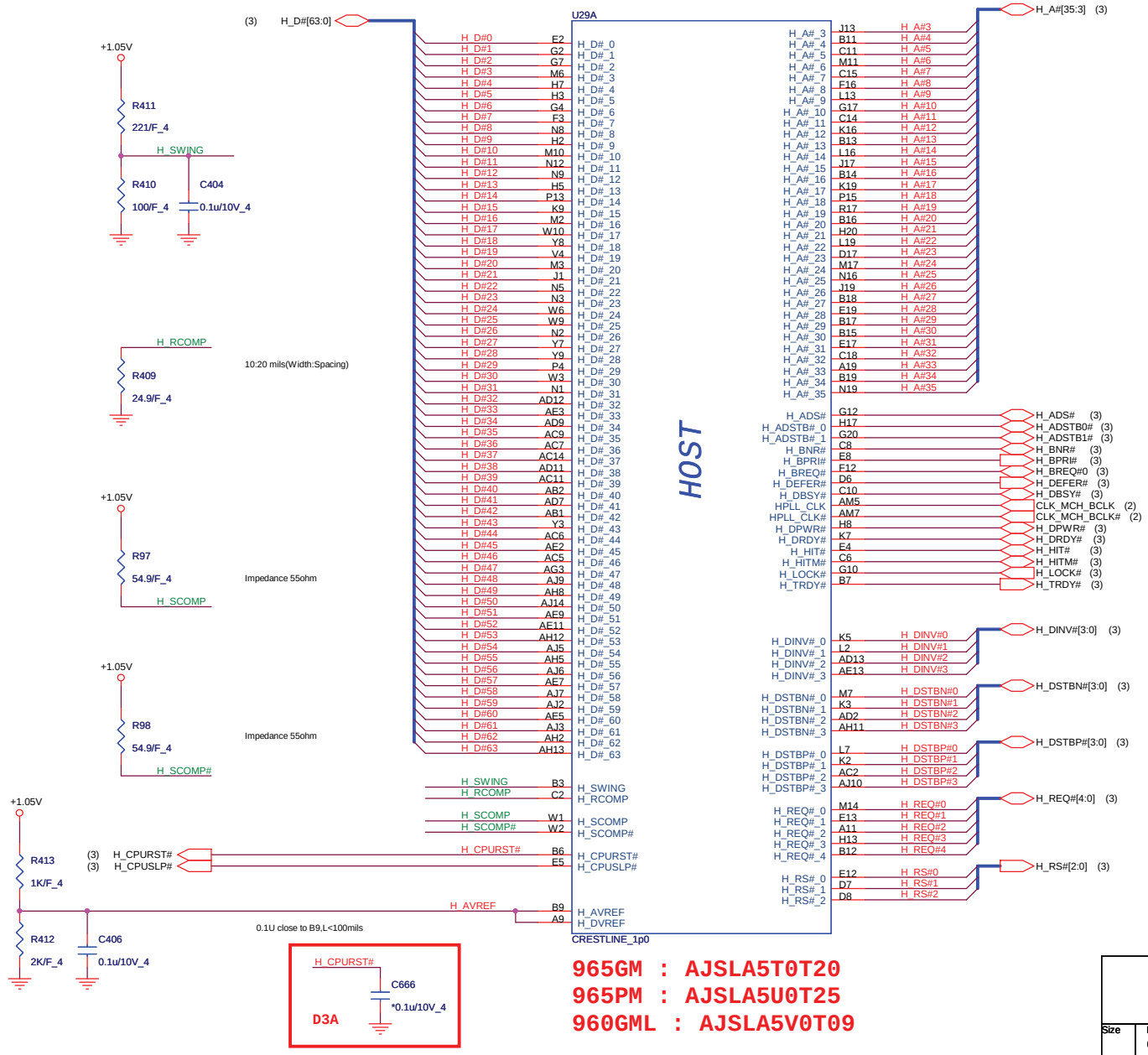

CPU(HOST)
U26A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
U26B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
Merom Ball-out Rev 1a
CPU Thermal monitor
Q10
RHU002N06
Q11
RHU002N06
U28
LM95245
ADDRESS: 98H
B2A
Q9
MMBT3904
CPU FAN
U27
G995
FANPWR = 1.6*VSET
FAN_CON
D3A
PU/PD (ITP700)
Thermal Trip
Q5
FDV301N
D3
*BAS316
Q6
MMBT3904
Quanta Computer Inc.
PROJECT : TE1
CPU(1 of 2)/FAN/Thermal
Wednesday, January 23, 2008
Sheet 3 of 41

CPU(Power)



Quanta Computer Inc.		
PROJECT : TE1		
Size	Document Number	Rev
	CPU(2 of 2)	1A
Date: Wednesday, January 23, 2008	Sheet 4 of 41	

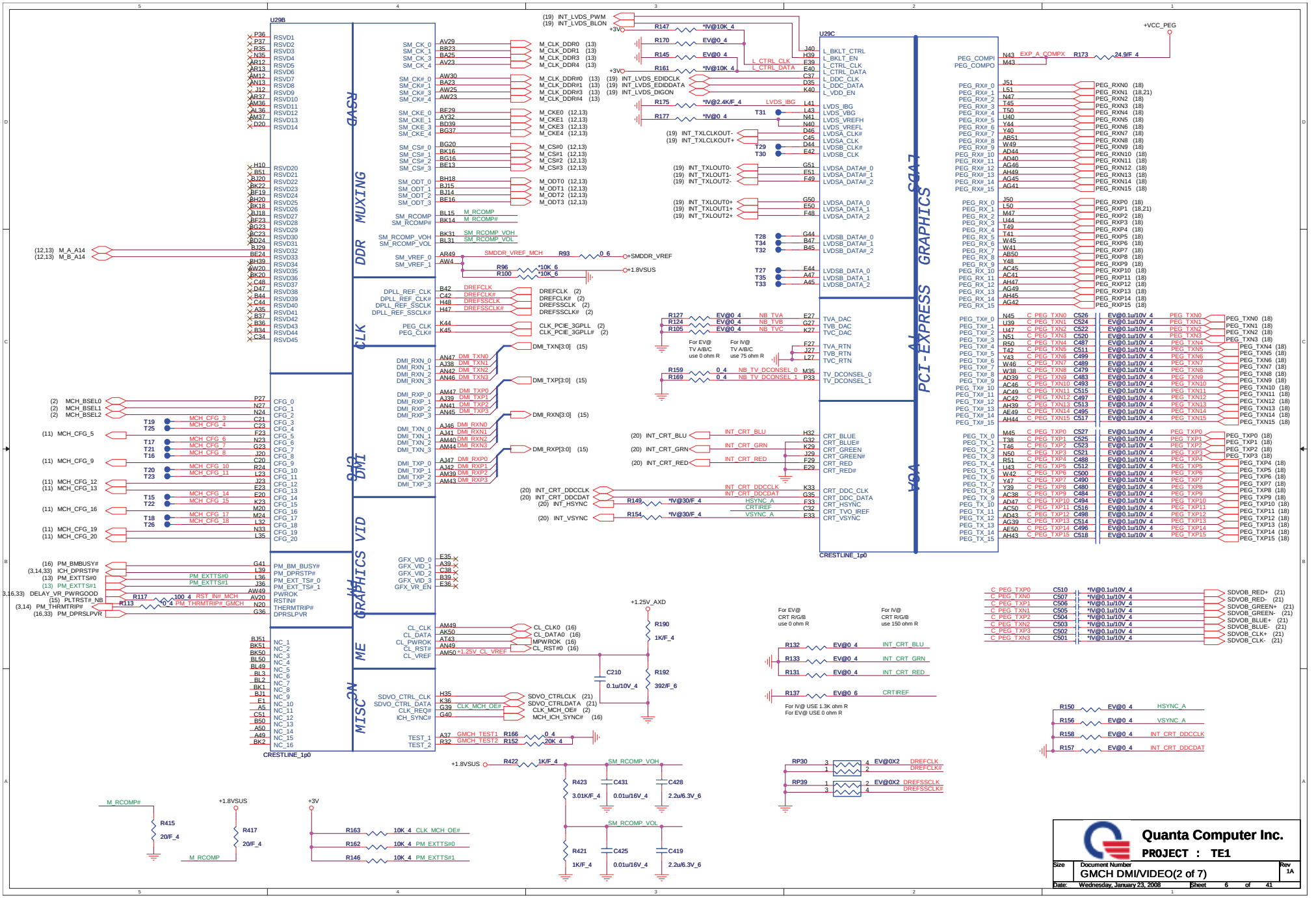
NB(HOST)



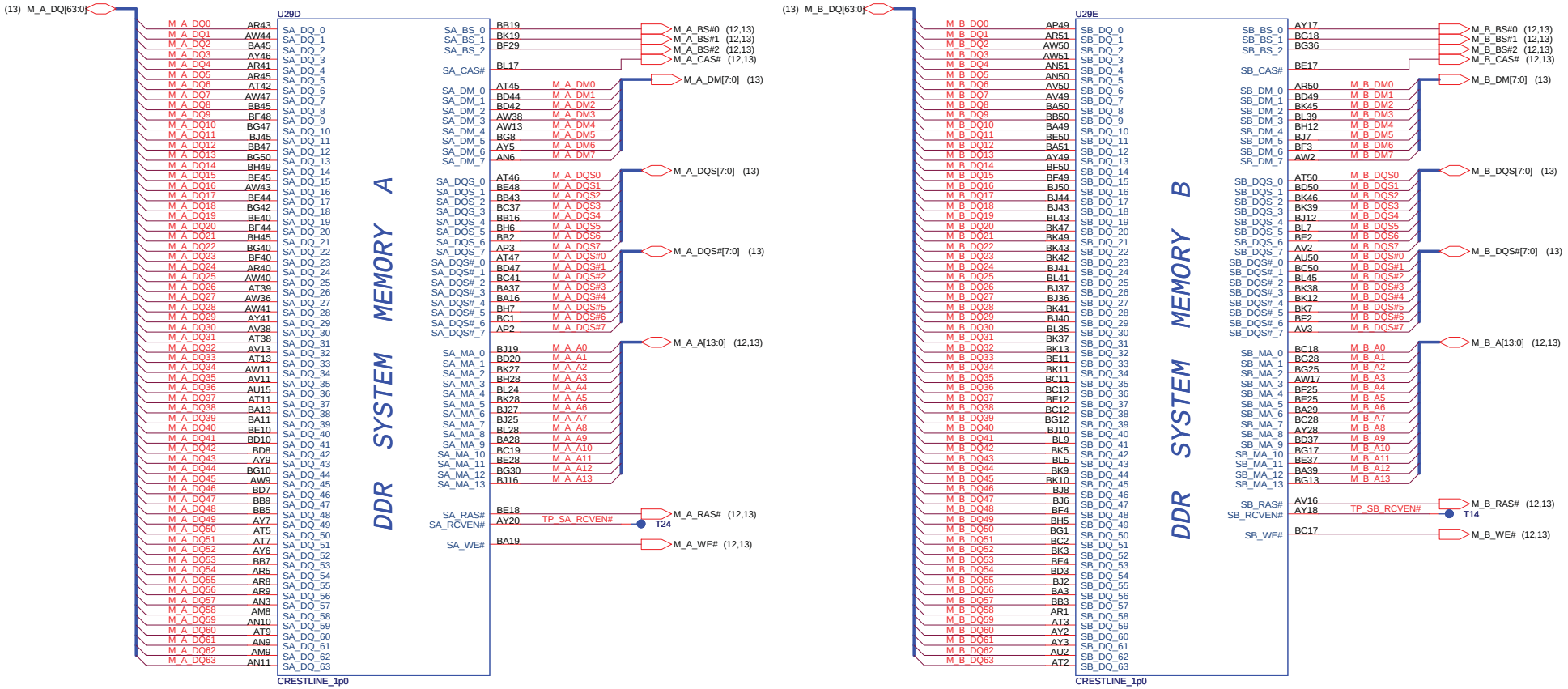
965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GML : AJSLA5V0T09

Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A
Date: Wednesday, January 23, 2008	Sheet 5 of 41	

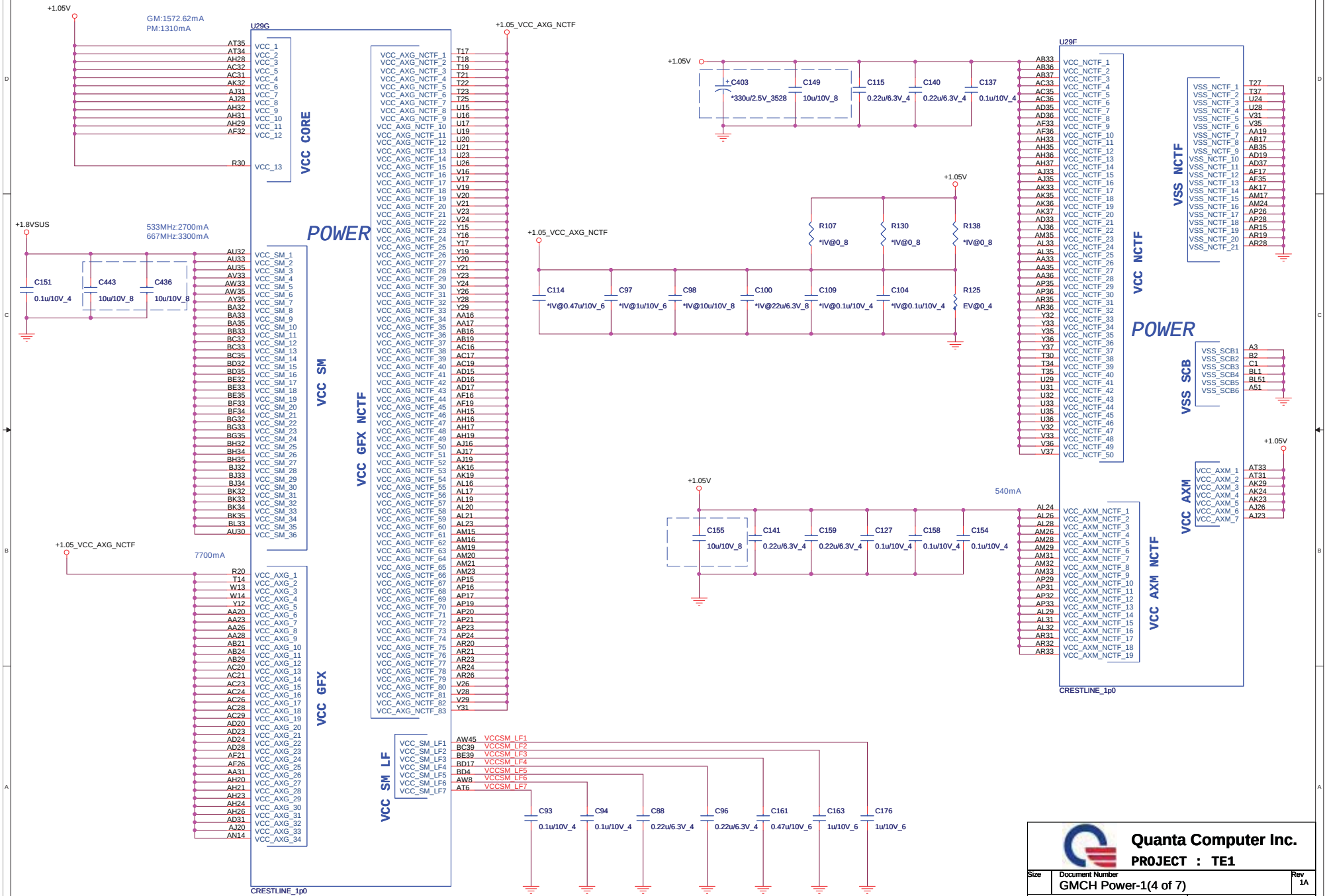

U29B
CRESTLINE_1p0
U29C
CRESTLINE_1p0
Quanta Computer Inc.
PROJECT : TE1
GMCH DMI/VIDEO(2 of 7)
Size
Document Number
Rev 1A
Date: Wednesday, January 23, 2008
Sheet 6 of 41

NB(Memory controller)

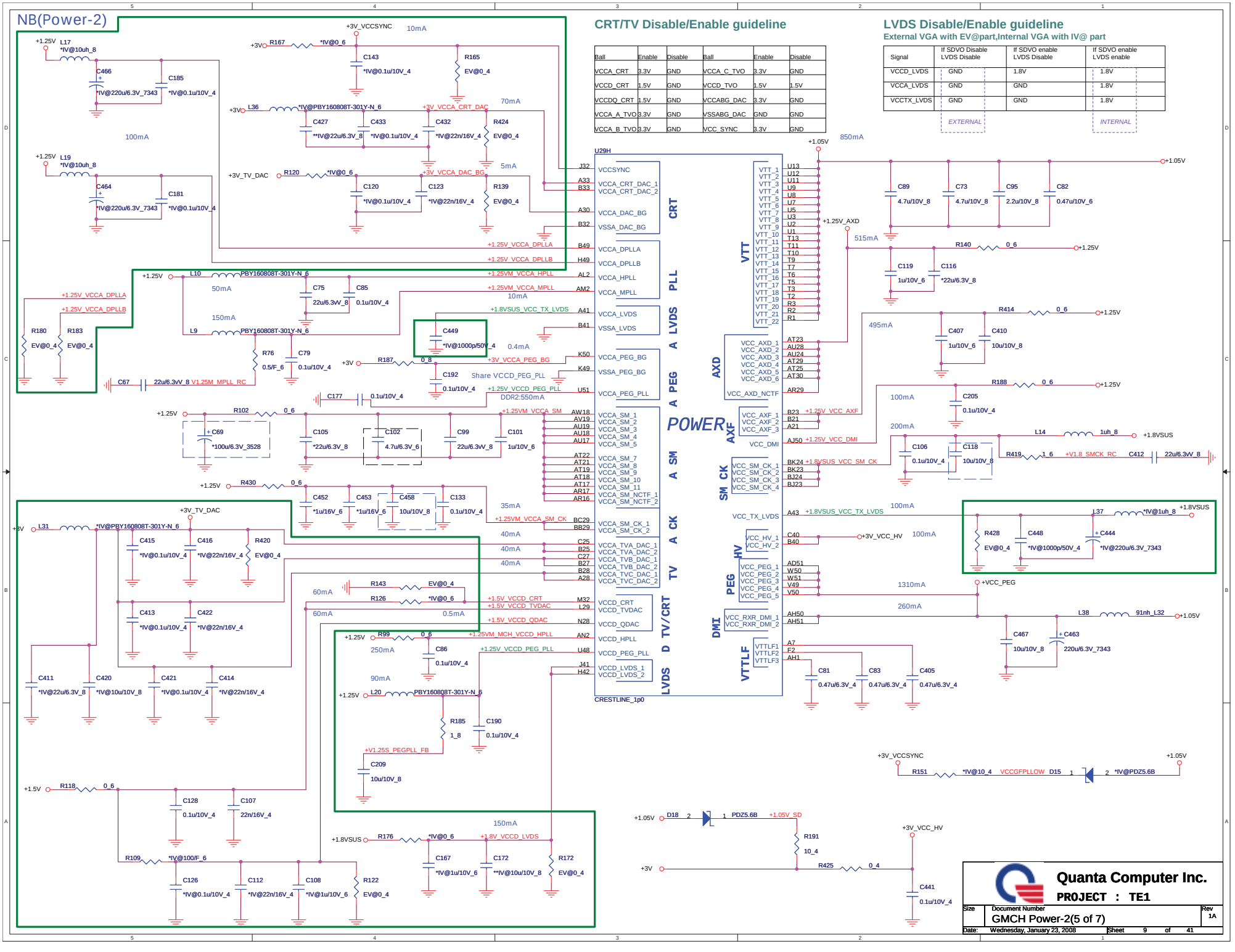


Quanta Computer Inc.		
PROJECT : TE1		
Size	Document Number: MCH DDR(3 of 7)	Rev: 1A
Date: Wednesday, January 23, 2008	Sheet 7 of 41	

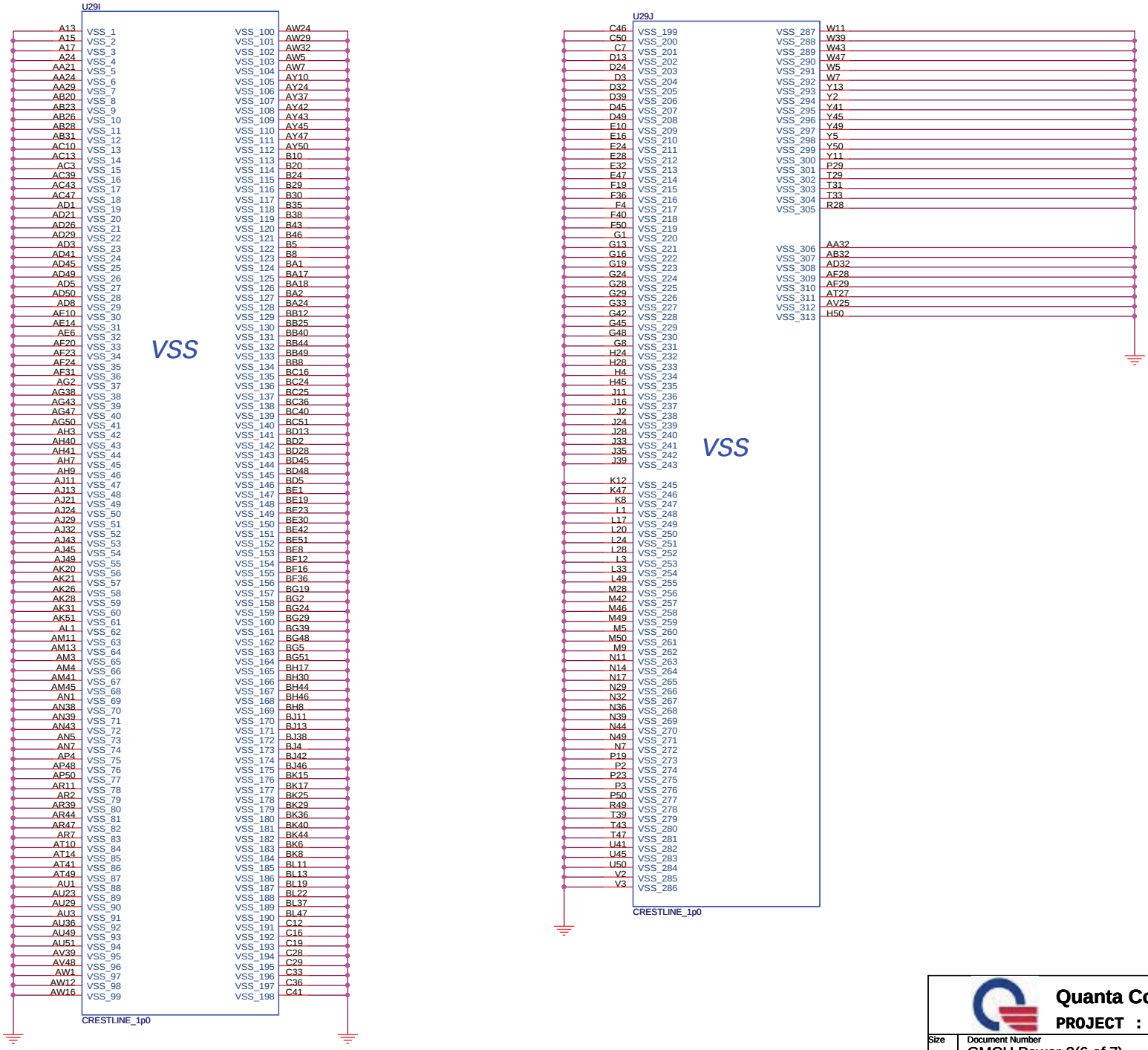
NB(Power-1)



Quanta Computer Inc.		
PROJECT : TE1		
Size	Document Number: GMCH Power-1(4 of 7)	Rev: 1A
Date: Wednesday, January 23, 2008	Sheet 8 of 41	


NB(Power-2)
CRT/TV Disable/Enable guideline
LVDS Disable/Enable guideline
External VGA with EV@part,Internal VGA with IV@ part
U29H
CRESTLINE_1p0
POWER
Quanta Computer Inc.
PROJECT : TE1
GMCH Power-2(5 of 7)
Wednesday, January 23, 2008

NB(Power-3)



Quanta Computer Inc.	
PROJECT : TE1	
Size	Document Number: GMCH Power-3(6 of 7) — Rev: 1A
Date: Wednesday, January 23, 2008	Sheet 10 of 41

Strap table(base on checklist Ver1.6)

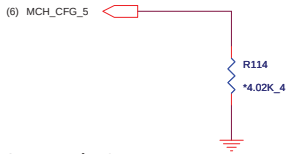
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

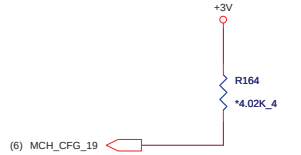
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

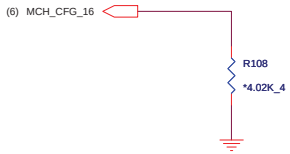
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

SDVO Present

Strap define at External HDMI control page

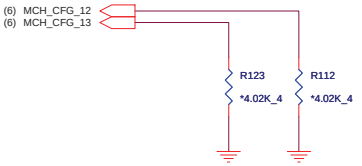
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO andPCIE are operating simultaneously via the PEG port



Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A
Date: Wednesday, January 23, 2008	Sheet 11 of 41	

DDR2 Dual channel A/B PU

M_A_A[13..0] → M_A_A[13..0] (7,13)

M_B_A[13..0] → M_B_A[13..0] (7,13)

DDRII A CHANNEL

+SMDDR_VTERM

C148 C165 C121 C132 C183 C174 C162 C147 C142 C194 C193 C195 C134

0.1u/10V_4

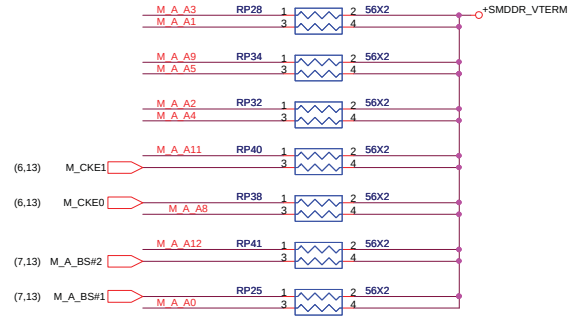
DDRII B CHANNEL

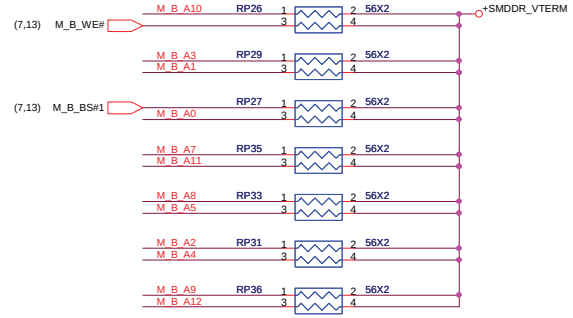
+SMDDR_VTERM

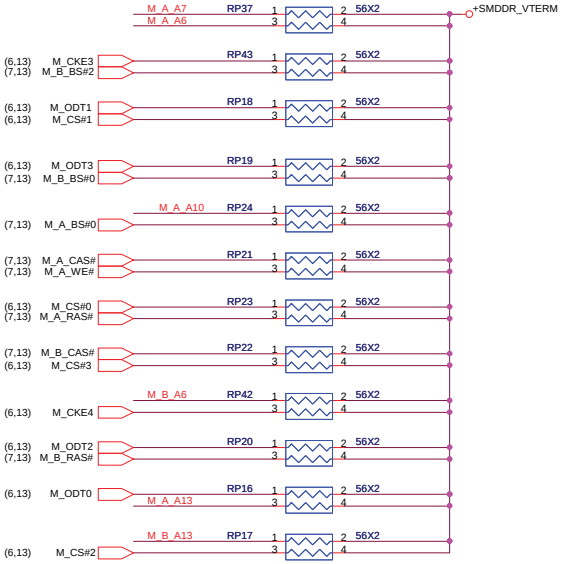
C202 C171 C124 C139 C125 C196 C203 C169 C160 C144 C178 C199 C152

0.1u/10V_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM







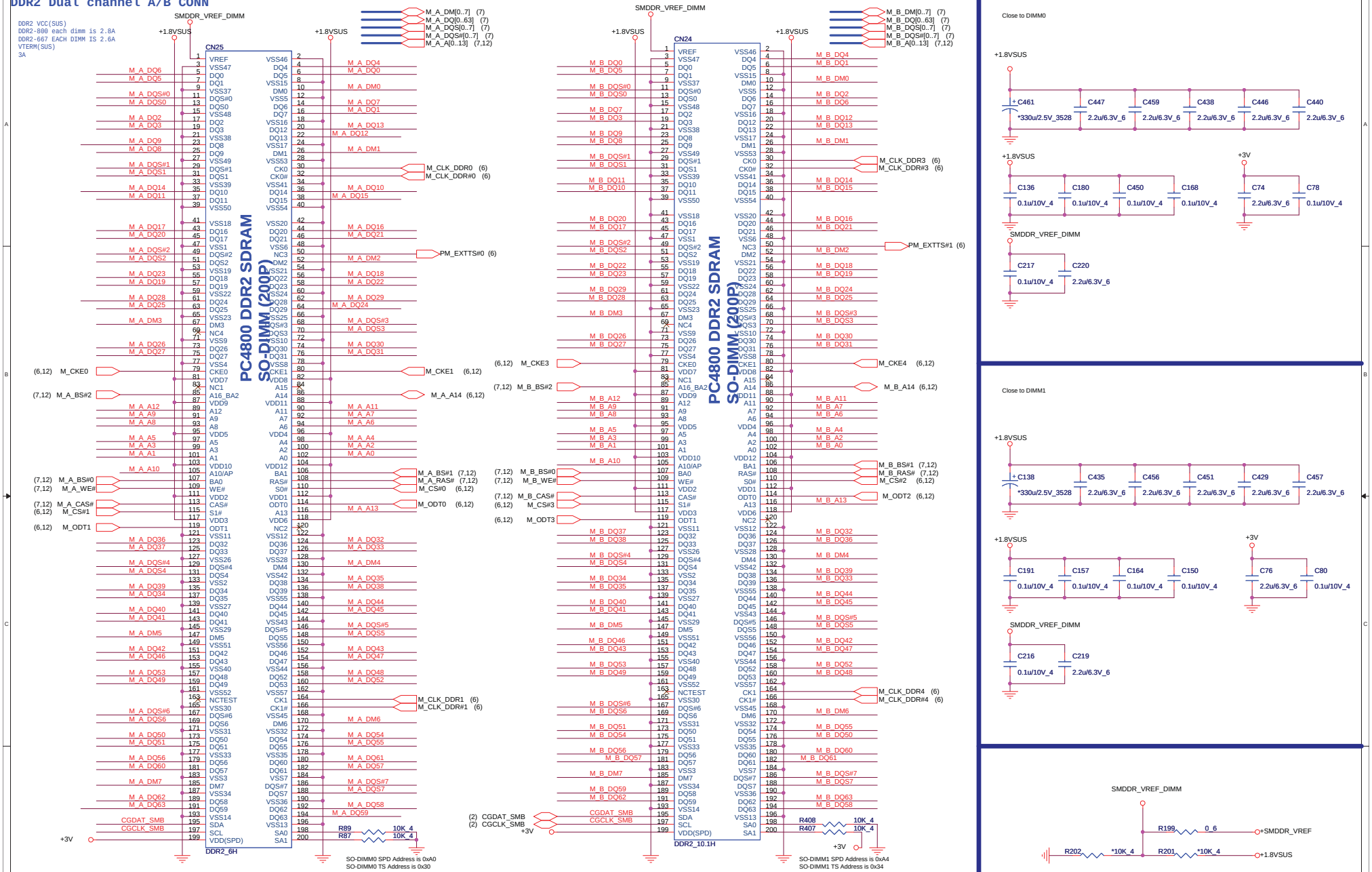
Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	DDR RES. ARRAY	1A
Date: Wednesday, January 23, 2008	Sheet 12 of 41	

DDR2 Dual channel A/B CONN

DDR2 VCC(SUS)
DDR2-800 each dimm is 2.8A
DDR2-667 EACH DIMM IS 2.6A
VTERM(SUS)
3A



H: 6mm

CLOCK 0,1
CKE 0,1

H: 10.1mm

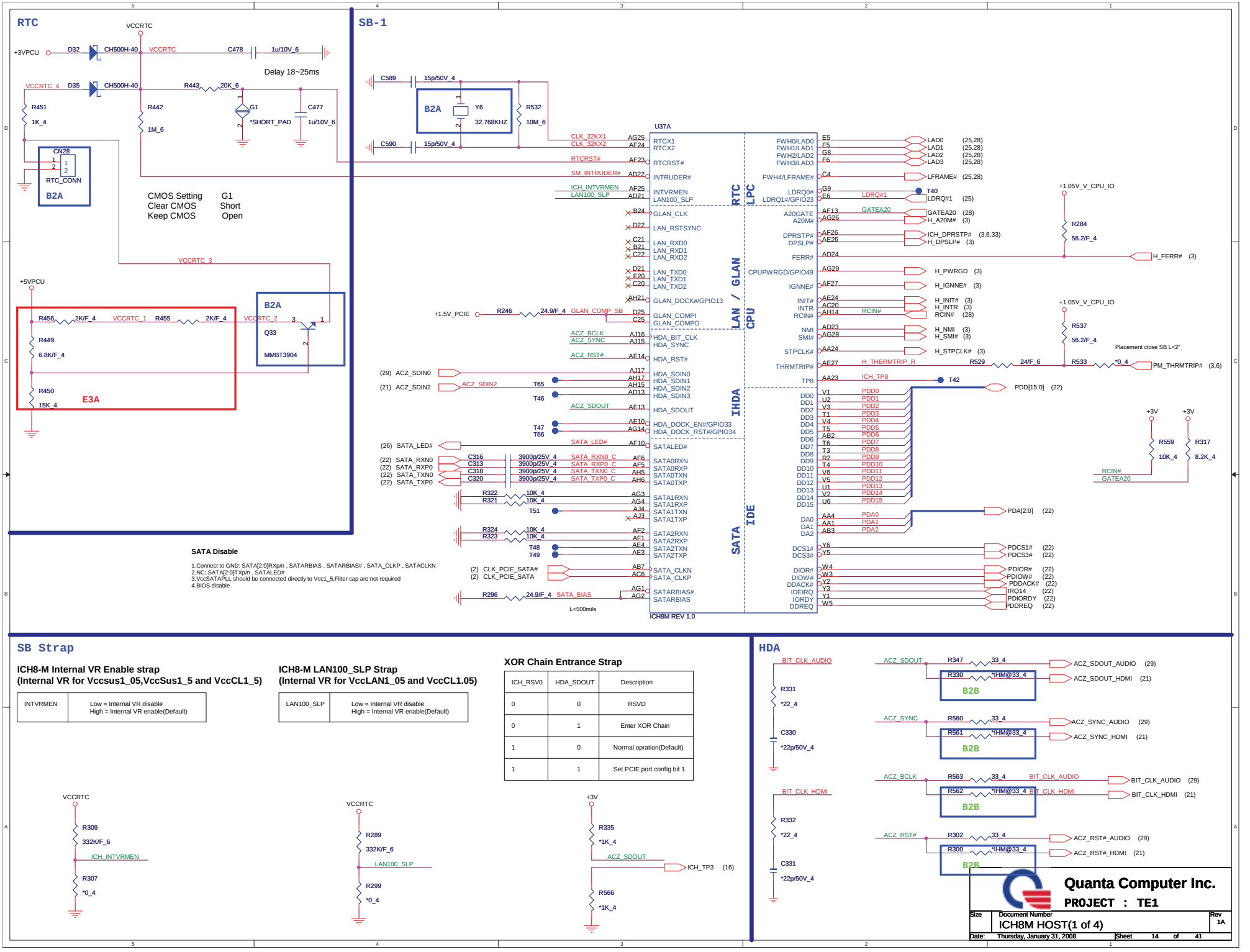
CLOCK 3,4
CKE 2,3

Close to DIMM0

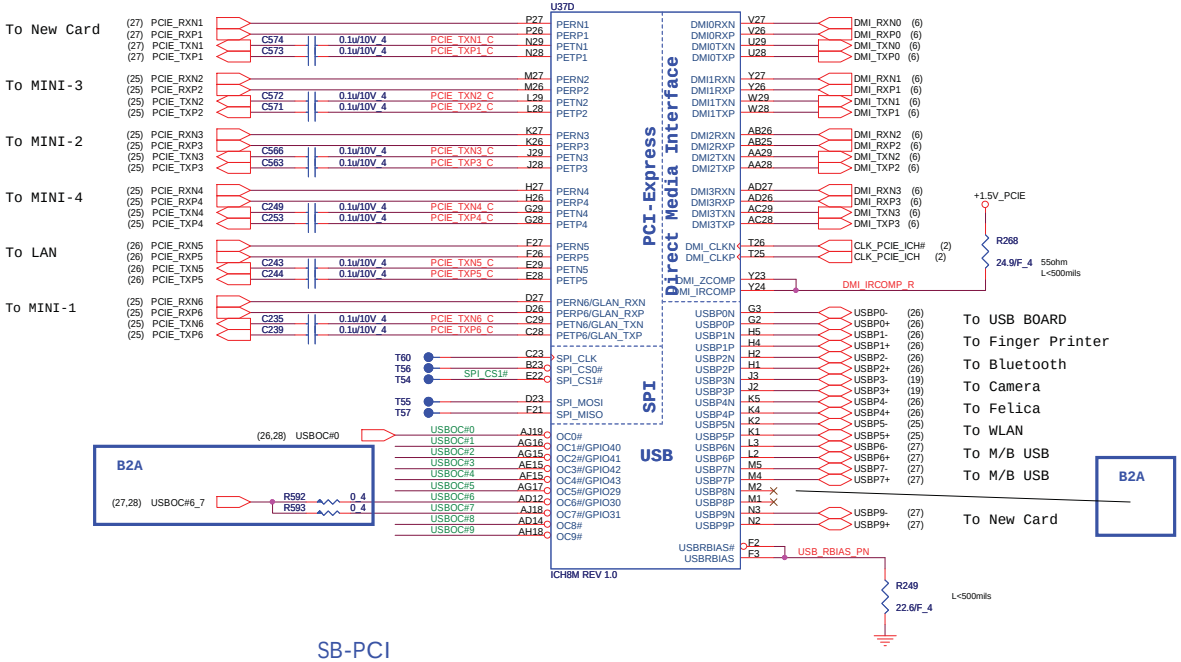
Close to DIMM1

Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	DDR SO-DIMM(200P)	1A
Date: Wednesday, January 23, 2008	Sheet 13 of 41	


RTC
VCCRTC
+3VPCU
D32
CH500H-40
C478
1u/10V_6
Delay 18~25ms
VCCRTC_4
D35
R443
20K_6
R451
1K_4
R442
1M_6
G1
*SHORT_PAD
C477
1u/10V_6
CN28
RTC_CONN
B2A
CMOS Setting
Clear CMOS
Keep CMOS
G1
Short
Open
VCCRTC_3
+5VPCU
R456
2K/F_4
VCCRTC_1
R455
2K/F_4
VCCRTC_2
Q33
MMBT3904
R449
6.8K/F_4
R450
15K_4
E3A
SB-1
C589
15p/50V_4
B2A
Y6
32.768KHZ
R532
10M_6
C590
15p/50V_4
U37A
CLK_32KX1
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
+1.5V_PCIE
R246
24.9/F_4
GLAN_COMP_SB
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH8M REV 1.0
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0 (25,28)
LAD1 (25,28)
LAD2 (25,28)
LAD3 (25,28)
LFRAME# (25,28)
LDRQ#1
LDRQ#1 (25)
GATEA20
GATEA20 (28)
H_A20M# (3)
ICH_DPRSTP# (3,6,33)
H_DPSLP# (3)
H_FERR# (3)
H_PWRGD (3)
H_IGNNE# (3)
H_INIT# (3)
H_INTR (3)
RCIN# (28)
H_NMI (3)
H_SMI# (3)
H_STPCLK# (3)
H_THERMTRIP_R
R529
24/F_6
ICH_TP8
T42
PDD[15:0] (22)
PDA[2:0] (22)
PDCS1# (22)
PDCS3# (22)
PDIOR# (22)
PDIOW# (22)
PDDACK# (22)
IRQ14 (22)
PDIORDY (22)
PDDREQ (22)
+1.05V_V_CPU_IO
R284
56.2/F_4
R537
56.2/F_4
Placement close SB L<2"
R533
*0_4
PM_THRMTRIP# (3,6)
+3V
R559
10K_4
R317
8.2K_4
RCIN#
GATEA20
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN2
ACZ_SDOUT
SATA_LED#
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_BIAS
L<500mils
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATA Disable
1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable
SB Strap
ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)
INTVRMEN
Low = Internal VR disable
High = Internal VR enable(Default)
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)
LAN100_SLP
Low = Internal VR disable
High = Internal VR enable(Default)
XOR Chain Entrance Strap
ICH_RSV0
HDA_SDOUT
Description
0
0
RSVD
0
1
Enter XOR Chain
1
0
Normal opration(Default)
1
1
Set PCIE port config bit 1
R309
332K/F_6
ICH_INTVRMEN
R307
*0_4
R289
332K/F_6
LAN100_SLP
R299
*0_4
R335
*1K_4
ACZ_SDOUT
ICH_TP3 (16)
R566
*1K_4
HDA
BIT_CLK_AUDIO
R331
*22_4
C330
*22p/50V_4
BIT_CLK_HDMI
R332
*22_4
C331
*22p/50V_4
ACZ_SDOUT
R347
33_4
R330
*IHM@33_4
B2B
ACZ_SDOUT_AUDIO (29)
ACZ_SDOUT_HDMI (21)
ACZ_SYNC
R560
33_4
R561
*IHM@33_4
B2B
ACZ_SYNC_AUDIO (29)
ACZ_SYNC_HDMI (21)
ACZ_BCLK
R563
33_4
R562
*IHM@33_4
B2B
BIT_CLK_AUDIO (29)
BIT_CLK_HDMI (21)
ACZ_RST#
R302
33_4
R300
*IHM@33_4
B2B
ACZ_RST#_AUDIO (29)
ACZ_RST#_HDMI (21)
Quanta Computer Inc.
PROJECT : TE1
Size
Document Number
ICH8M HOST(1 of 4)
Rev
1A
Date: Thursday, January 31, 2008
Sheet 14 of 41

SB-PCIE/USB/DMI



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R469 *1K_4

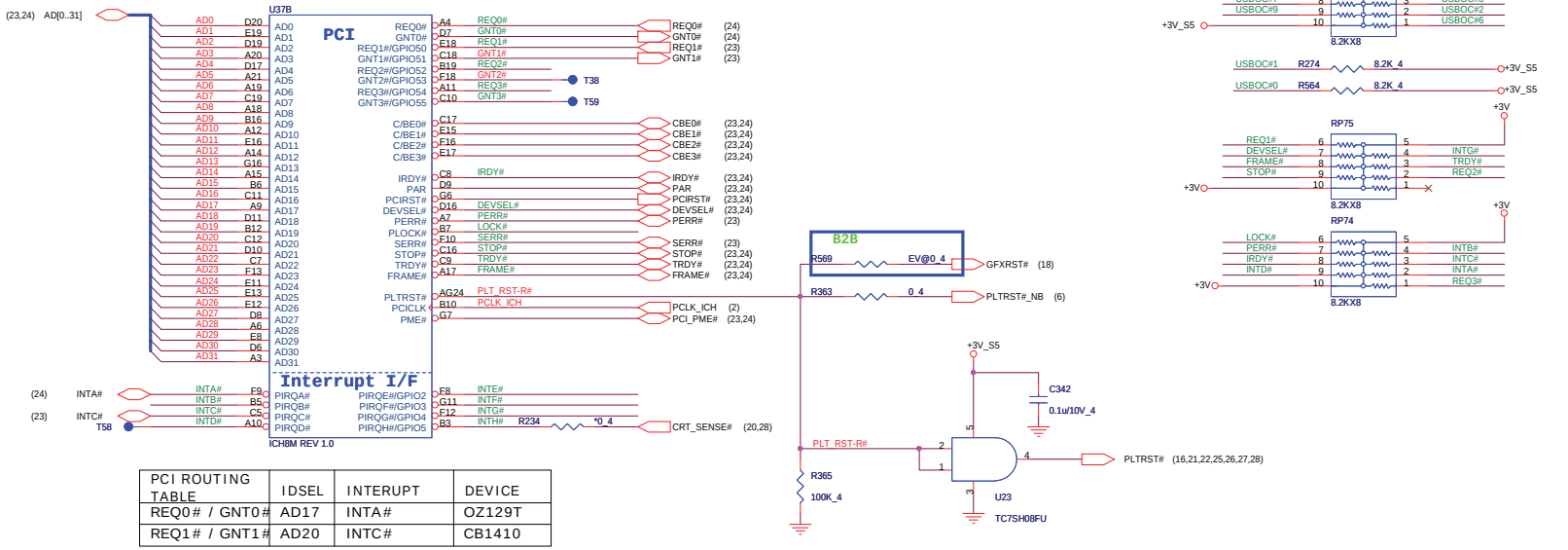
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

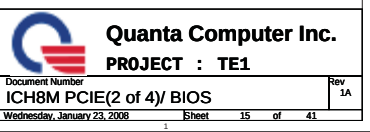
SPI_CS1# R467 *1K_4

GNT0# R244 *1K_4

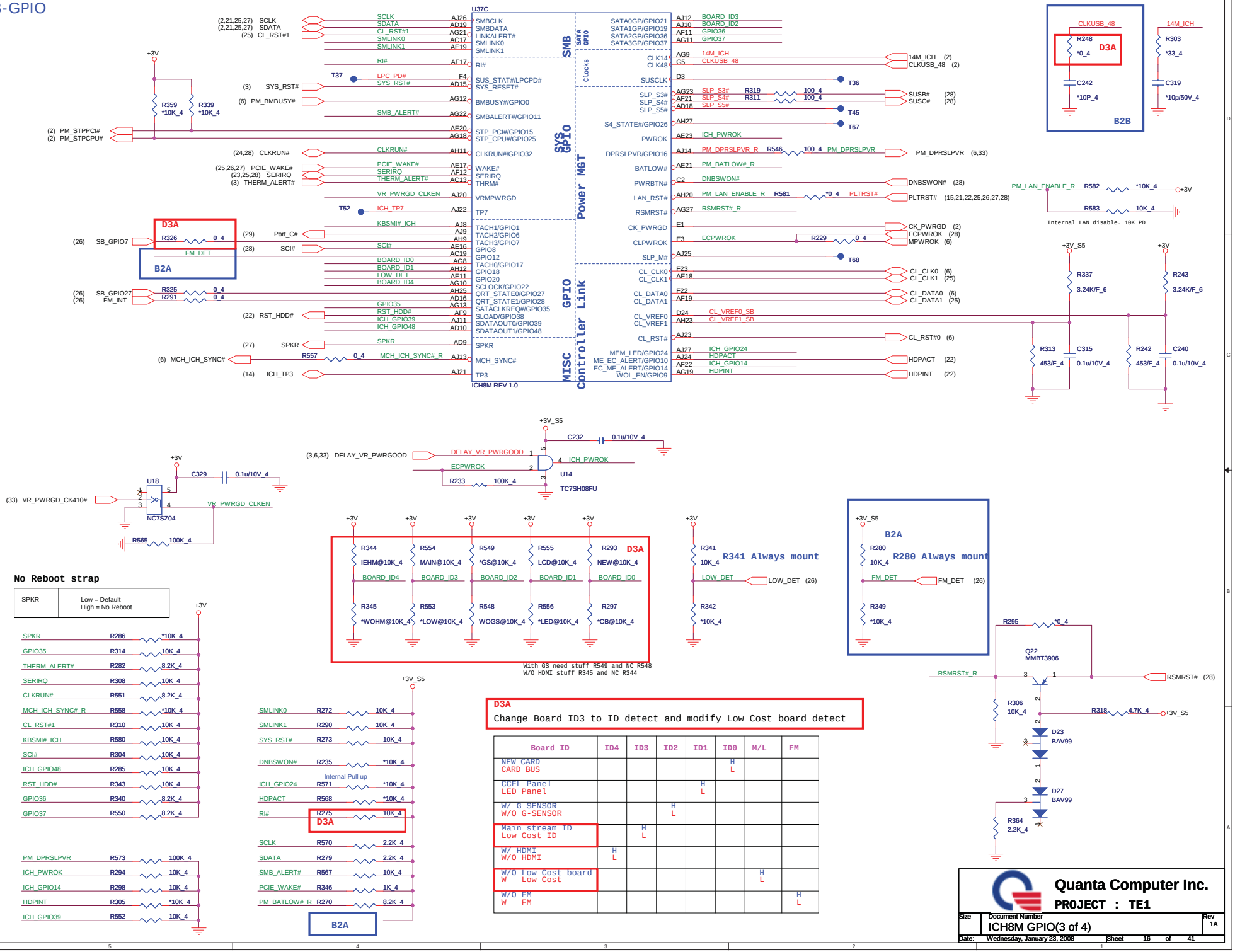
SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD20	INTC#	CB1410



SB-GPIO



No Reboot strap

SPKR	Low = Default High = No Reboot

D3A

Change Board ID3 to ID detect and modify Low Cost board detect

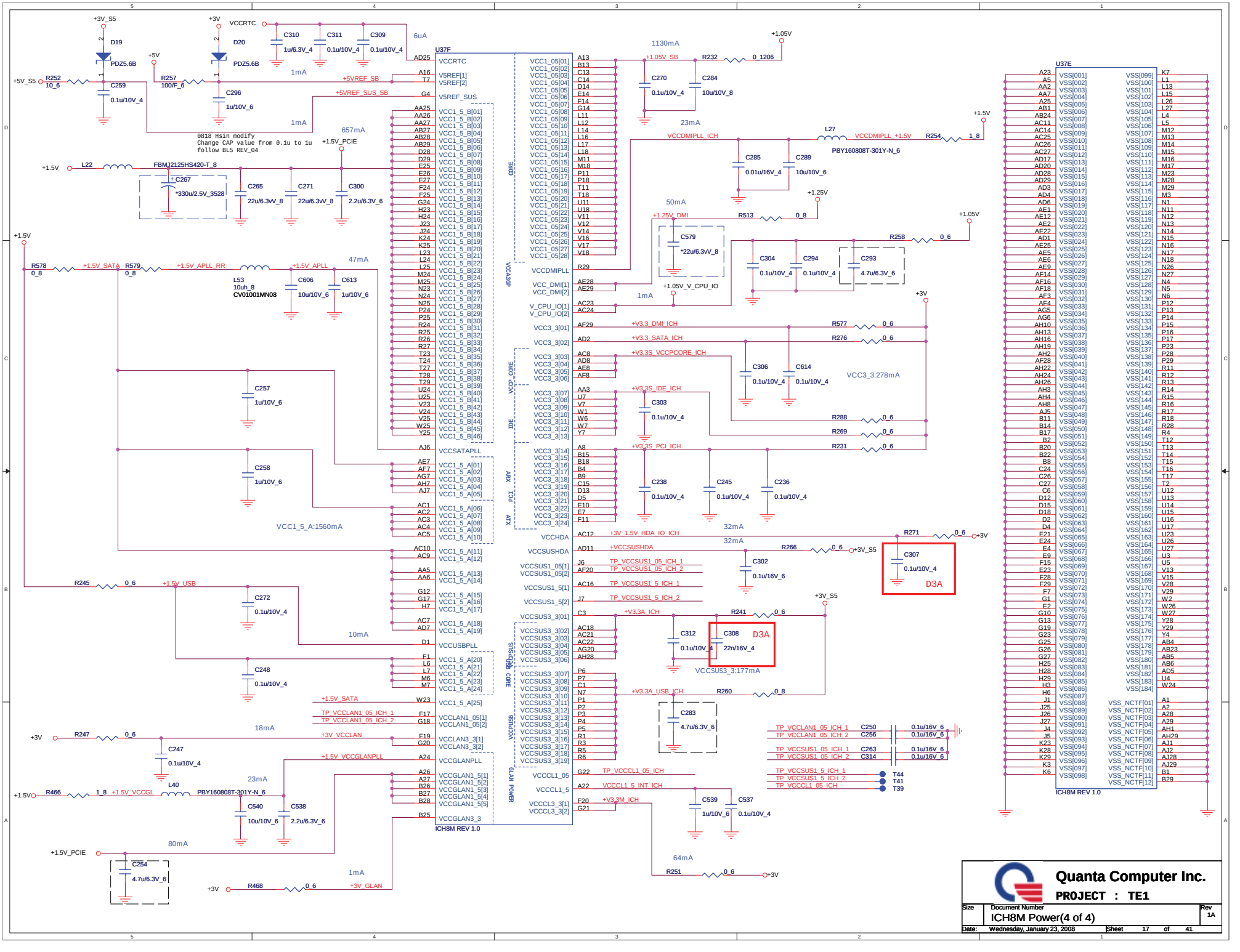
Board ID	ID4	ID3	ID2	ID1	ID0	M/L	FM
NEW CARD CARD BUS					H L		
CCFL Panel LED Panel				H L			
W/ G-SENSOR W/O G-SENSOR			H L				
Main Stream ID Low Cost ID		H L					
W/ HDMI W/O HDMI	H L						
W/O Low Cost board W Low Cost						H L	
W/O FM W FM							H L

Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	1A

Date: Wednesday, January 23, 2008 Sheet 16 of 41


U37F
ICH8M REV 1.0
U37E
ICH8M REV 1.0
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCCSATAPLL
VCCUSBPLL
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
VCCHDA
VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
VCCSUS3_3[03]
VCCSUS3_3[04]
VCCSUS3_3[05]
VCCSUS3_3[06]
VCCSUS3_3[07]
VCCSUS3_3[08]
VCCSUS3_3[09]
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VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
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VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
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VCC1_5_A[02]
VCC1_5_A[03]
VCC1_5_A[04]
VCC1_5_A[05]
VCC1_5_A[06]
VCC1_5_A[07]
VCC1_5_A[08]
VCC1_5_A[09]
VCC1_5_A[10]
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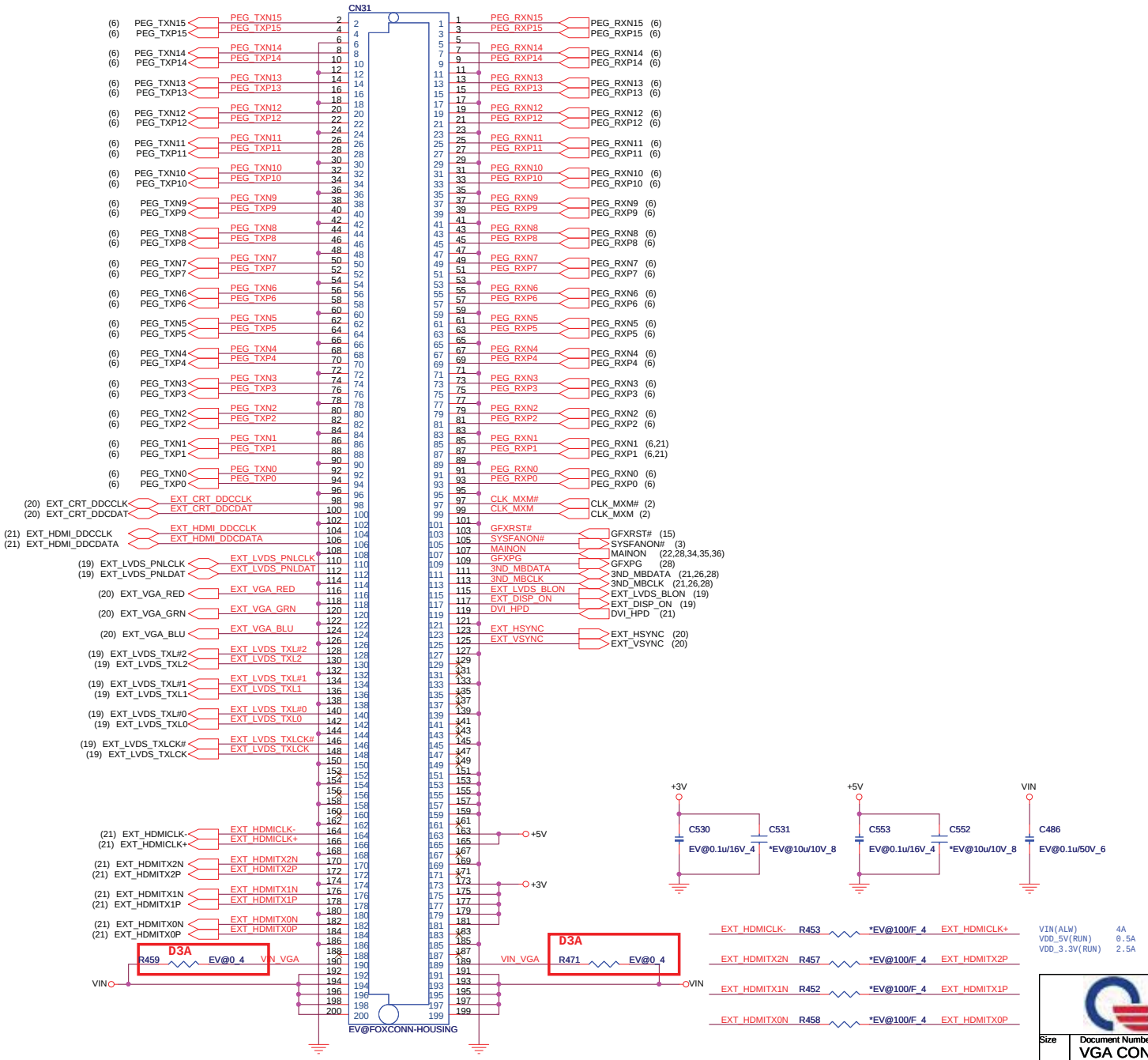
+3V_S5
+3V
+5V
+5V_S5
+1.5V
+1.5V_PCIE
+1.05V
+1.25V
D19
PDZ5.6B
D20
PDZ5.6B
R252 10_6
R257 100/F_6
C259 0.1u/10V_4
C296 1u/10V_6
C310 1u/6.3V_4
C311 0.1u/10V_4
C309 0.1u/10V_4
6uA
1mA
+5VREF_SB
+5VREF_SUS_SUS
0818 Hsin modify
Change CAP value from 0.1u to 1u
follow BL5 REV_04
657mA
L22 FBMJ2125HS420-T_8
C267 *330u/2.5V_3528
C265 22u/6.3V_8
C271 22u/6.3V_8
C300 2.2u/6.3V_6
R578 0_8
R579 0_8
+1.5V_SATA
+1.5V_APLL_RR
+1.5V_APLL
47mA
L53 10uh_8 CV01001MN08
C606 10u/10V_6
C613 1u/10V_6
C257 1u/10V_6
C258 1u/10V_6
VCC1_5_A:1560mA
R245 0_6
+1.5V_USB
C272 0.1u/10V_4
10mA
C248 0.1u/10V_4
+1.5V_SATA
TP_VCCLAN1_05_ICH_1
TP_VCCLAN1_05_ICH_2
18mA
R247 0_6
+3V_VCCLAN
C247 0.1u/10V_4
+1.5V_VCCGLANPLL
23mA
R466 1_8
+1.5V_VCCGL
L40 PBY160808T-301Y-N_6
C540 10u/10V_6
C538 2.2u/6.3V_6
80mA
+1.5V_PCIE
C254 4.7u/6.3V_6
1mA
R468 0_6
+3V_GLAN
1130mA
+1.05V_SB
R232 0_1206
C270 0.1u/10V_4
C284 10u/10V_8
23mA
VCCDMIPLL_ICH
L27 PBY160808T-301Y-N_6
VCCDMIPLL_+1.5V
R254 1_8
C285 0.01u/16V_4
C289 10u/10V_6
50mA
+1.25V_DMI
R513 0_8
C579 *22u/6.3V_8
1mA
+1.05V_V_CPU_IO
C304 0.1u/10V_4
C294 0.1u/10V_4
C293 4.7u/6.3V_6
R258 0_6
R577 0_6
+V3.3_DMI_ICH
+V3.3_SATA_ICH
R276 0_6
+V3.3S_VCCPCORE_ICH
C306 0.1u/10V_4
C614 0.1u/10V_4
VCC3_3:278mA
+V3.3S_IDE_ICH
C303 0.1u/10V_4
R288 0_6
R269 0_6
+V3.3S_PCI_ICH
R231 0_6
C238 0.1u/10V_4
C245 0.1u/10V_4
C236 0.1u/10V_4
32mA
+3V_1.5V_HDA_IO_ICH
R271 0_6
32mA
+VCCSUSHDA
R266 0_6
C307 0.1u/10V_4
D3A
TP_VCCSUS1_05_ICH_1
TP_VCCSUS1_05_ICH_2
C302 0.1u/16V_6
TP_VCCSUS1_5_ICH_1
TP_VCCSUS1_5_ICH_2
+V3.3A_ICH
R241 0_6
C312 0.1u/10V_4
C308 22n/16V_4
D3A
VCCSUS3_3:177mA
+V3.3A_USB_ICH
R260 0_8
C283 4.7u/6.3V_6
TP_VCCCL1_05_ICH
TP_VCCCL1_5_INT_ICH
+V3.3M_ICH
C539 1u/10V_6
C537 0.1u/10V_4
64mA
R251 0_6
C250 0.1u/16V_6
C256 0.1u/16V_6
C263 0.1u/16V_6
C314 0.1u/16V_6
T44
T41
T39
Quanta Computer Inc.
PROJECT : TE1
Size
Document Number
ICH8M Power(4 of 4)
Rev 1A
Date: Wednesday, January 23, 2008
Sheet 17 of 41

VGA/B conn

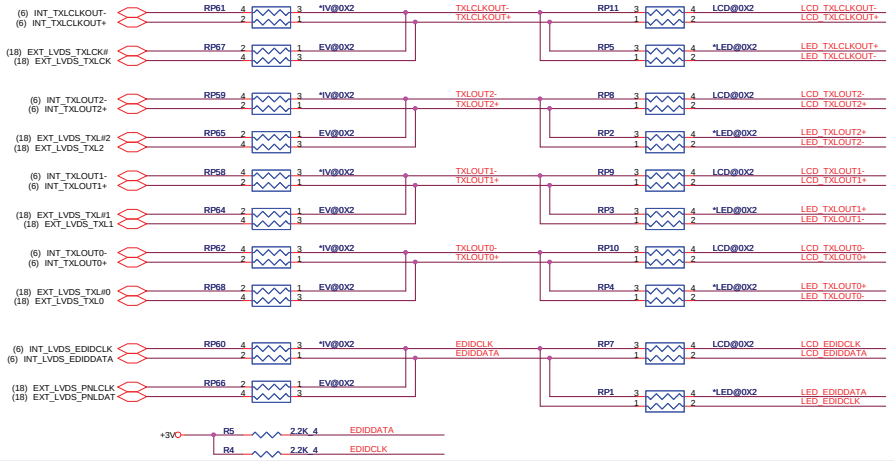


Quanta Computer Inc.

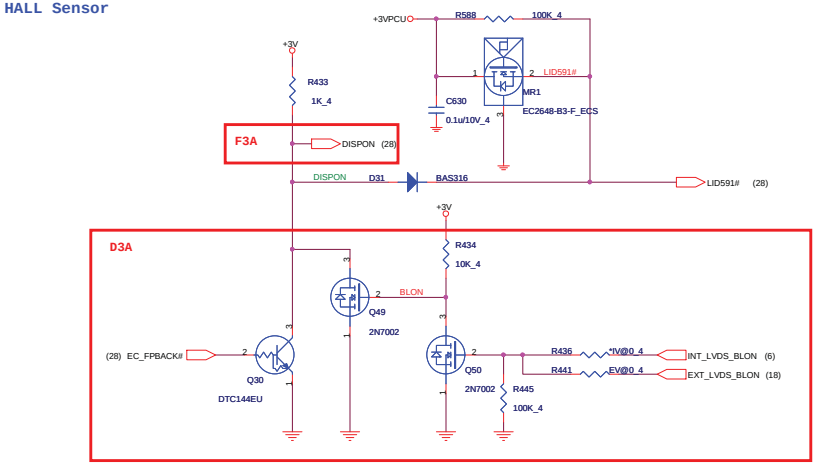
PROJECT : TE1

Size	Document Number	Rev
	VGA CONNECTOR	1A
Date: Wednesday, January 23, 2008	Sheet 18 of 41	

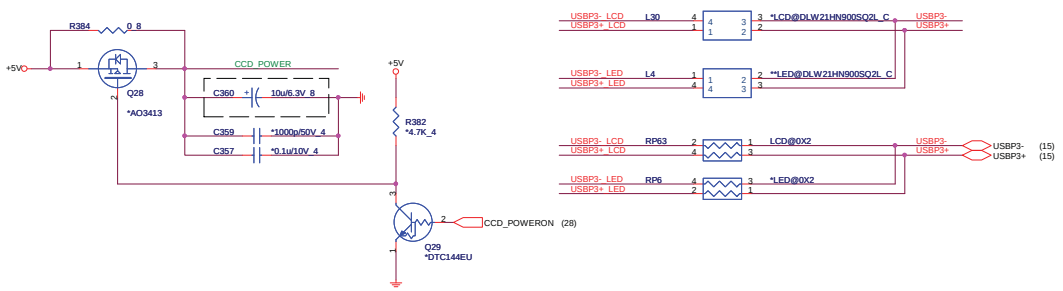
Panel source



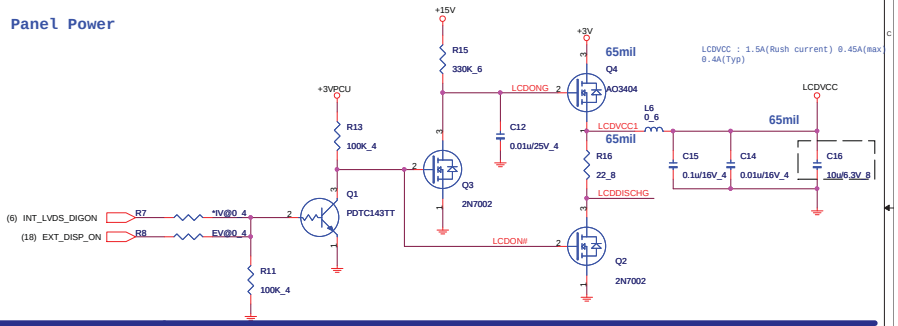
HALL Sensor



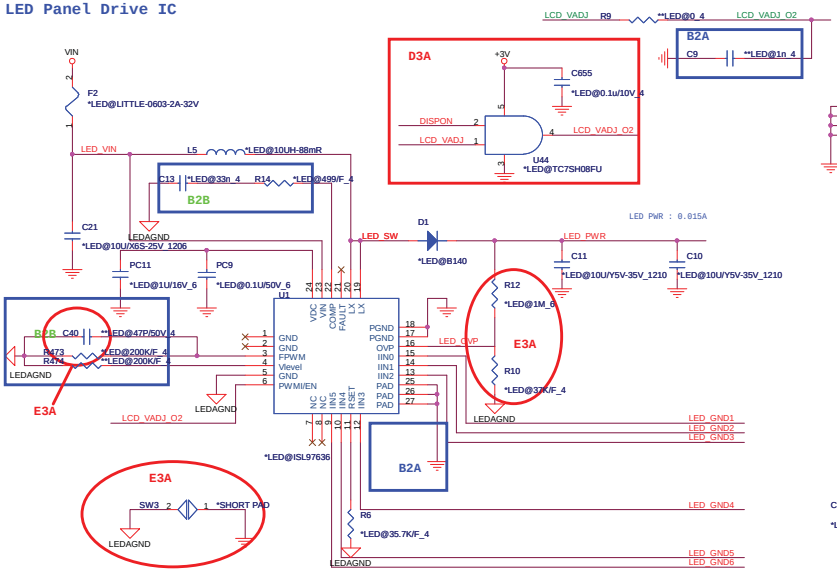
CAMERA Module



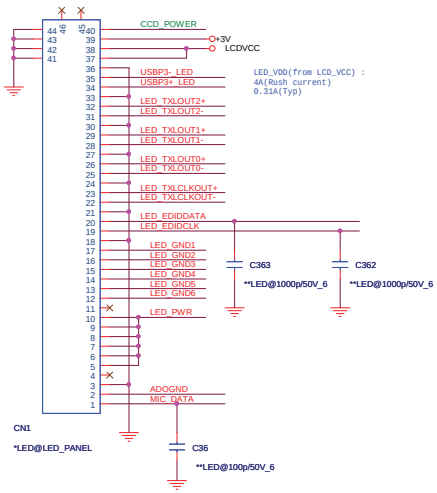
Panel Power



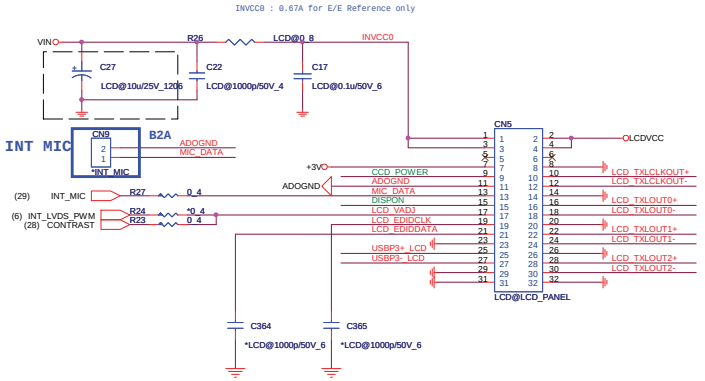
LED Panel Drive IC



TOSHIBA LED Panel Module

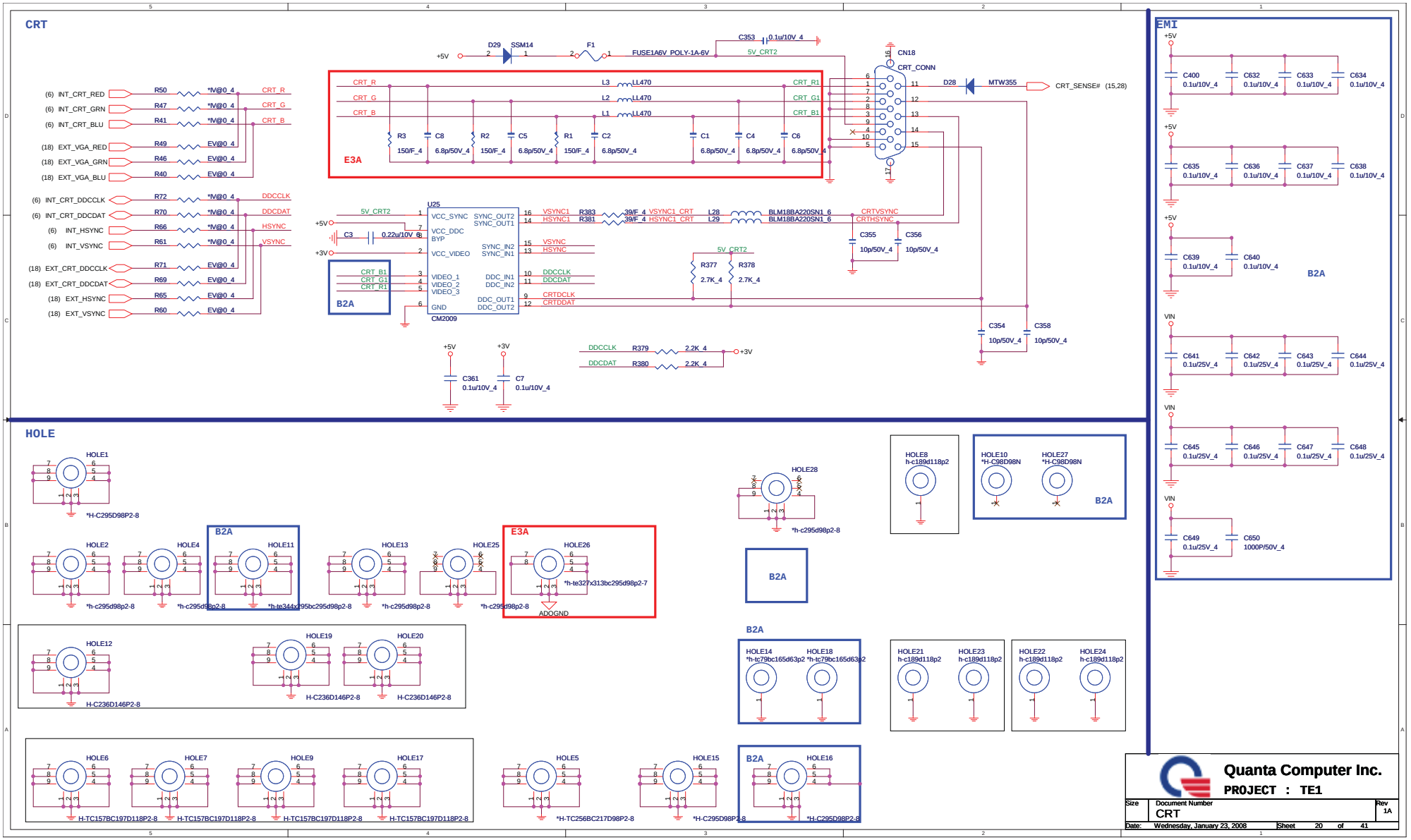


LCD Panel Module



Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	LCD/CRT/LID/CAMERA	1A
Date: Wednesday, February 13, 2008	Sheet 19 of 41	


CRT
(6) INT_CRT_RED
(6) INT_CRT_GRN
(6) INT_CRT_BLU
(18) EXT_VGA_RED
(18) EXT_VGA_GRN
(18) EXT_VGA_BLU
R50
R47
R41
R49
R46
R40
*IV@0_4
EV@0_4
CRT_R
CRT_G
CRT_B
(6) INT_CRT_DDCCLK
(6) INT_CRT_DDCDAT
(6) INT_HSYNC
(6) INT_VSYNC
(18) EXT_CRT_DDCCLK
(18) EXT_CRT_DDCDAT
(18) EXT_HSYNC
(18) EXT_VSYNC
R72
R70
R66
R61
R71
R69
R65
R60
DDCCLK
DDCDAT
HSYNC
VSYNC
+5V
D29
SSM14
F1
FUSE1A6V_POLY-1A-6V
5V_CRT2
C353
0.1u/10V_4
CN18
CRT_CONN
D28
MTW355
CRT_SENSE# (15,28)
E3A
L3
L2
L1
LL470
CRT_R1
CRT_G1
CRT_B1
R3
R2
R1
C8
C5
C2
C1
C4
C6
150/F_4
6.8p/50V_4
U25
VCC_SYNC
VCC_DDC
BYP
VCC_VIDEO
VIDEO_1
VIDEO_2
VIDEO_3
GND
SYNC_OUT2
SYNC_OUT1
SYNC_IN2
SYNC_IN1
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
CM2009
VSYNC1
HSYNC1
R383
R381
39/F_4
VSYNC1_CRT
HSYNC1_CRT
L28
L29
BLM18BA220SN1_6
CRTVSYNC
CRTHSYNC
VSYNC
HSYNC
DDCCLK
DDCDAT
CRTDCLK
CRTDDAT
+3V
C3
0.22u/10V_6
B2A
R377
R378
2.7K_4
C355
C356
C354
C358
10p/50V_4
C361
C7
0.1u/10V_4
R379
R380
2.2K_4
EMI
C400
C632
C633
C634
C635
C636
C637
C638
C639
C640
C641
C642
C643
C644
C645
C646
C647
C648
C649
C650
0.1u/10V_4
0.1u/25V_4
1000P/50V_4
VIN
HOLE
HOLE1
HOLE2
HOLE4
HOLE11
HOLE13
HOLE25
HOLE26
HOLE28
HOLE12
HOLE19
HOLE20
HOLE6
HOLE7
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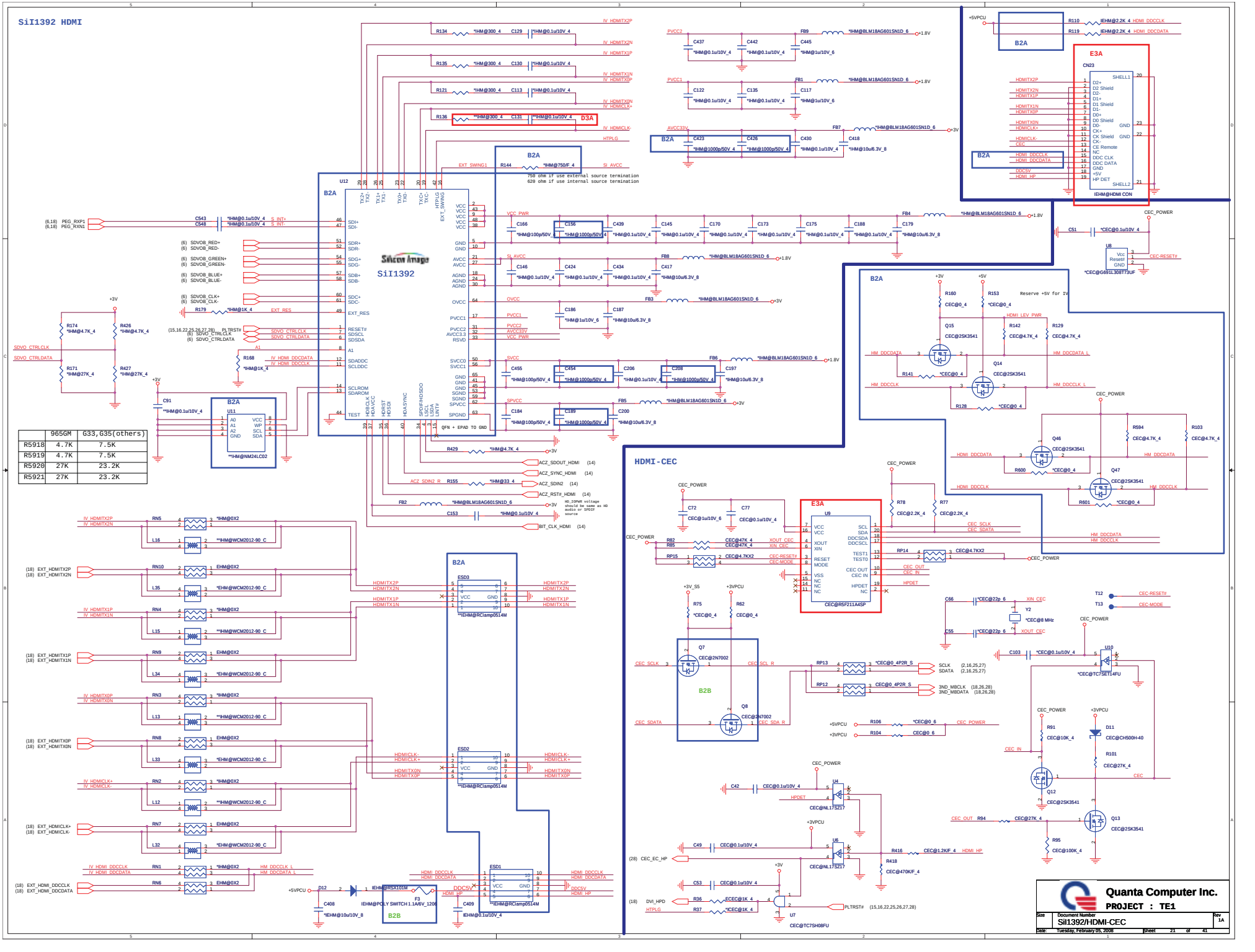
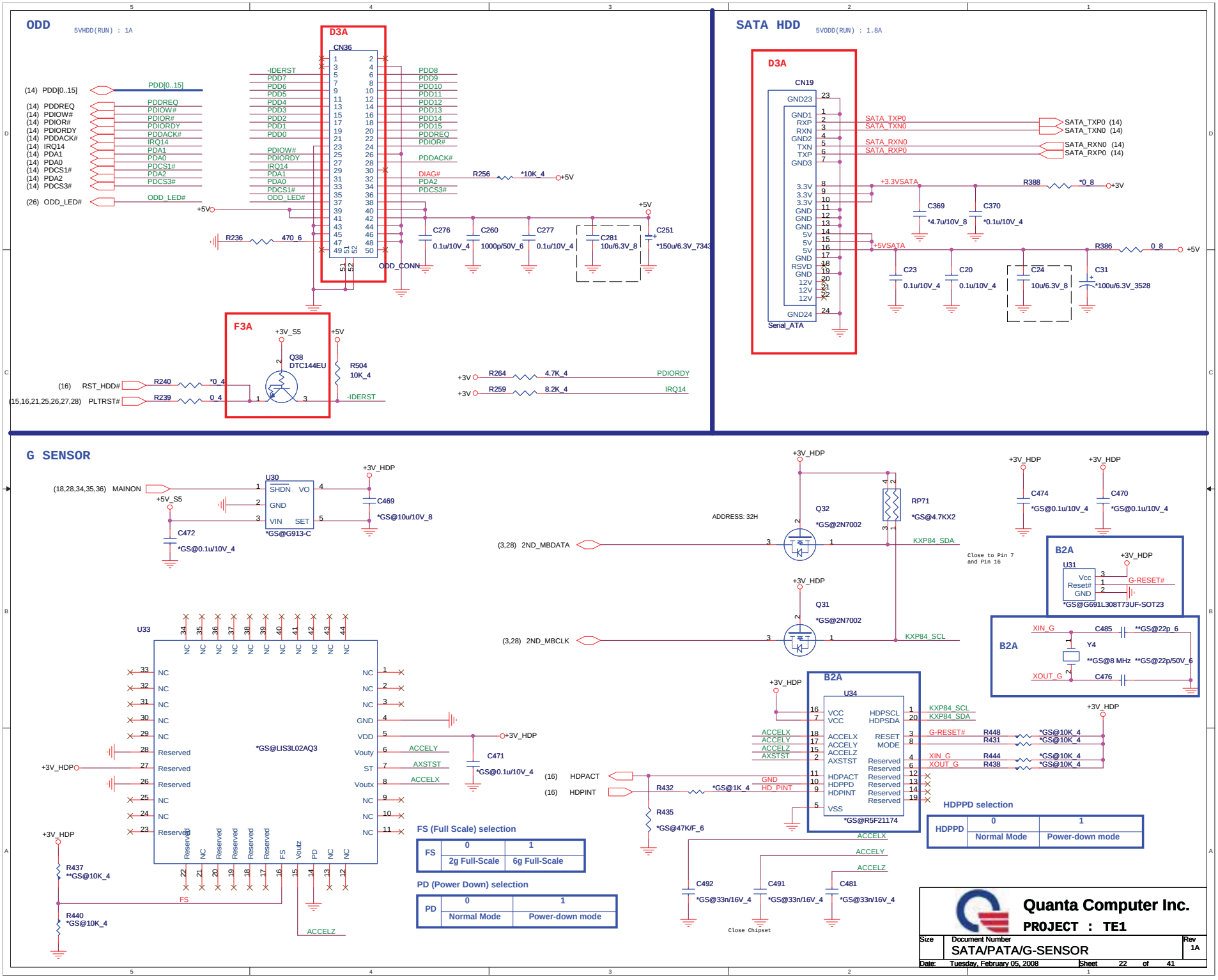
HOLE23
HOLE22
HOLE24
*H-C295D98P2-8
*h-c295d98p2-8
*h-te344x295bc295d98p2-8
*h-te327x313bc295d98p2-7
ADOGND
H-C236D146P2-8
H-TC157BC197D118P2-8
*H-TC256BC217D98P2-8
*H-C295D98P2-8
h-c189d118p2
*H-C98D98N
*h-tc790bc165d63p2
Quanta Computer Inc.
PROJECT : TE1
Size
Document Number
CRT
Rev
1A
Date: Wednesday, January 23, 2008
Sheet 20 of 41



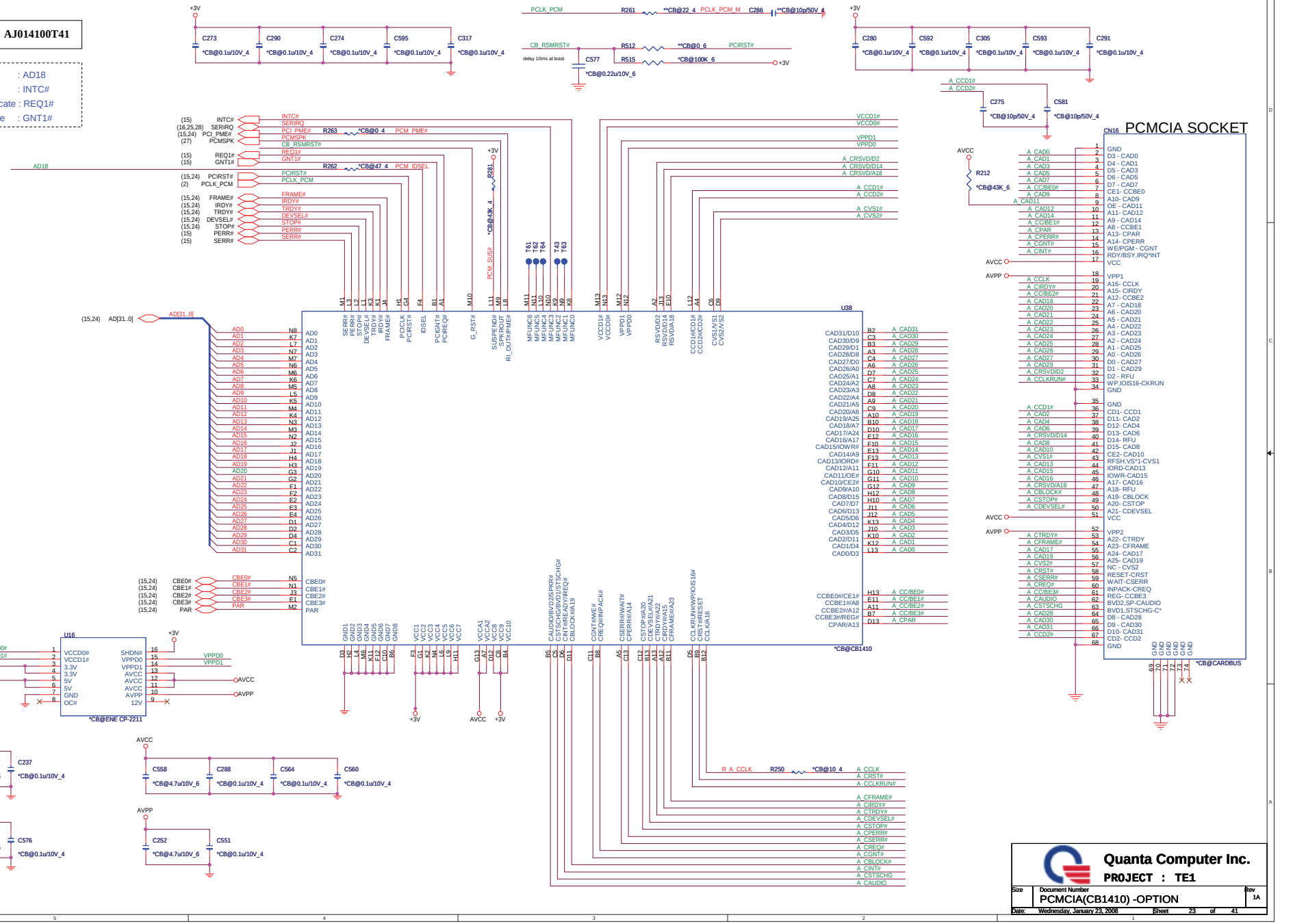
	965GM	G33,635(others)
R5918	4.7K	7.5K
R5919	4.7K	7.5K
R5920	27K	23.2K
R5921	27K	23.2K


ODD
5VHDD(RUN) : 1A
D3A
CN36
(14) PDD[0..15]
PDD[0..15]
(14) PDDREQ
(14) PDIOW#
(14) PDIOR#
(14) PDIORDY
(14) PDDACK#
(14) IRQ14
(14) PDA1
(14) PDA0
(14) PDCS1#
(14) PDA2
(14) PDCS3#
(26) ODD_LED#
-IDERST
PDIOW#
PDIORDY
PDDACK#
DIAG#
R256 *10K_4 +5V
R236 470_6
C276 0.1u/10V_4
C260 1000p/50V_6
C277 0.1u/10V_4
C281 10u/6.3V_8
C251 *150u/6.3V_7343
ODD_CONN
F3A
Q38 DTC144EU
R504 10K_4
(16) RST_HDD# R240 *0_4
(15,16,21,25,26,27,28) PLTRST# R239 0_4
R264 4.7K_4 PDIORDY
R259 8.2K_4 IRQ14
SATA HDD
5VODD(RUN) : 1.8A
D3A
CN19
Serial_ATA
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
SATA_TXP0 (14)
SATA_TXN0 (14)
SATA_RXN0 (14)
SATA_RXP0 (14)
+3.3VSATA
+5VSATA
R388 *0_8 +3V
R386 0_8 +5V
C369 *4.7u/10V_8
C370 *0.1u/10V_4
C23 0.1u/10V_4
C20 0.1u/10V_4
C24 10u/6.3V_8
C31 *100u/6.3V_3528
G SENSOR
(18,28,34,35,36) MAINON
U30
SHDN VO GND VIN SET
*GS@G913-C
C469 *GS@10u/10V_8
C472 *GS@0.1u/10V_4
U33
*GS@LIS3L02AQ3
C471 *GS@0.1u/10V_4
ACCELY
AXSTST
ACCELX
ACCELZ
FS
R437 **GS@10K_4
R440 *GS@10K_4
FS (Full Scale) selection
FS | 0 | 1
2g Full-Scale | 6g Full-Scale
PD (Power Down) selection
PD | 0 | 1
Normal Mode | Power-down mode
ADDRESS: 32H
Q32 *GS@2N7002
Q31 *GS@2N7002
RP71 *GS@4.7KX2
(3,28) 2ND_MBDATA
(3,28) 2ND_MBCLK
KXP84_SDA
KXP84_SCL
Close to Pin 7 and Pin 16
C474 *GS@0.1u/10V_4
C470 *GS@0.1u/10V_4
B2A
U31
Vcc Reset# GND
G-RESET#
*GS@G691L308T73UF-SOT23
XIN_G
XOUT_G
Y4
**GS@8 MHz
C485 **GS@22p_6
C476 **GS@22p/50V_6
B2A
U34
VCC VCC HDPSCL HDPSDA
ACCELX ACCELY ACCELZ AXSTST
RESET MODE
Reserved Reserved Reserved Reserved
HDPACT HDPPD HDPINT VSS
*GS@R5F21174
(16) HDPACT
(16) HDPINT
R432 *GS@1K_4
R435 *GS@47K/F_6
GND HD_PINT
G-RESET# R448 R431 *GS@10K_4
XIN_G R444 *GS@10K_4
XOUT_G R438 *GS@10K_4
HDPPD selection
HDPPD | 0 | 1
Normal Mode | Power-down mode
C492 *GS@33n/16V_4
C491 *GS@33n/16V_4
C481 *GS@33n/16V_4
Close Chipset
Quanta Computer Inc.
PROJECT : TE1
Size
Document Number
SATA/PATA/G-SENSOR
Rev 1A
Date: Tuesday, February 05, 2008
Sheet 22 of 41

Cardbus

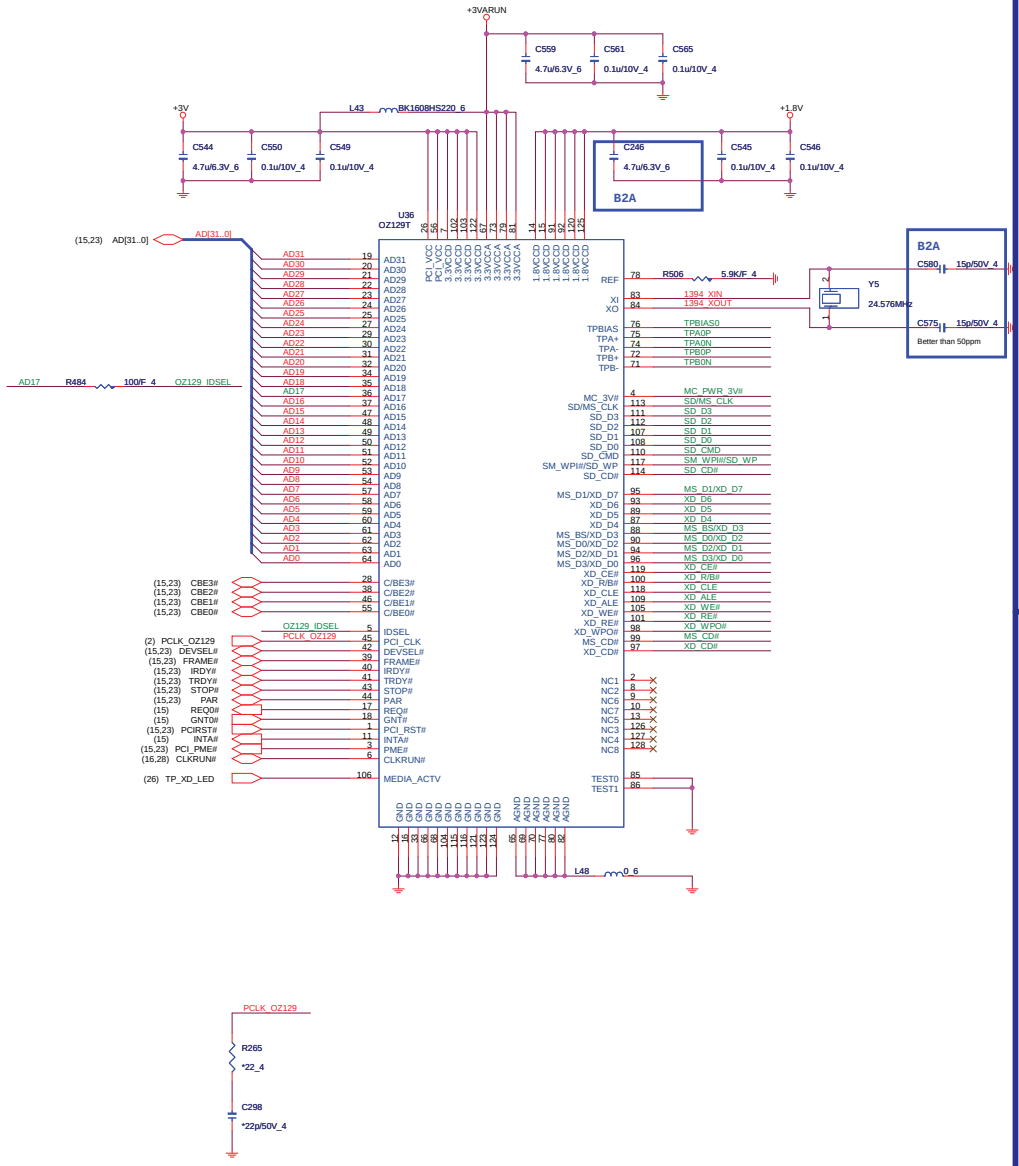
ENE1410	AJ014100T41

ID Select : AD18
Interrupt Pin : INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#

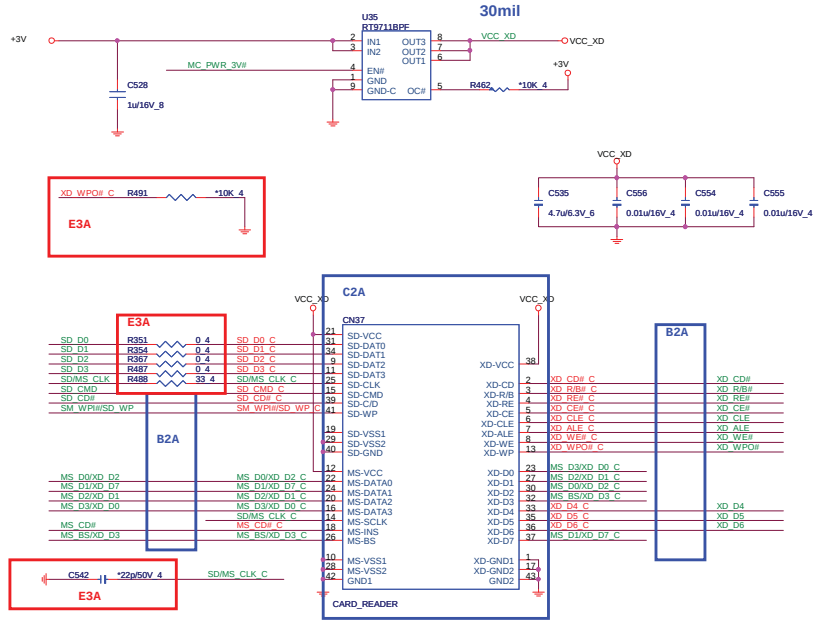


OZ129 for Cardreader+1394

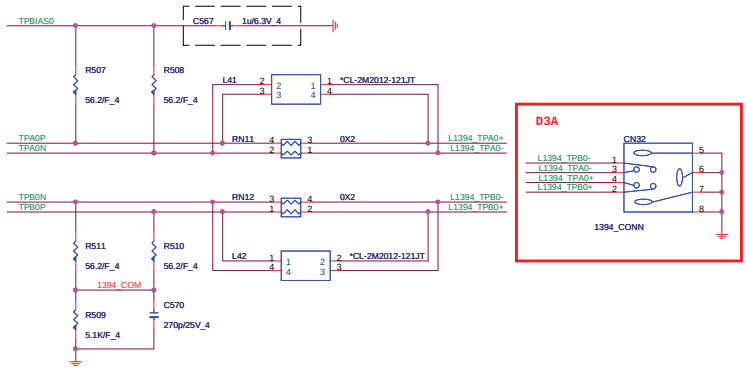
ID Select : AD17
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#



5 IN 1 Card reader



1394

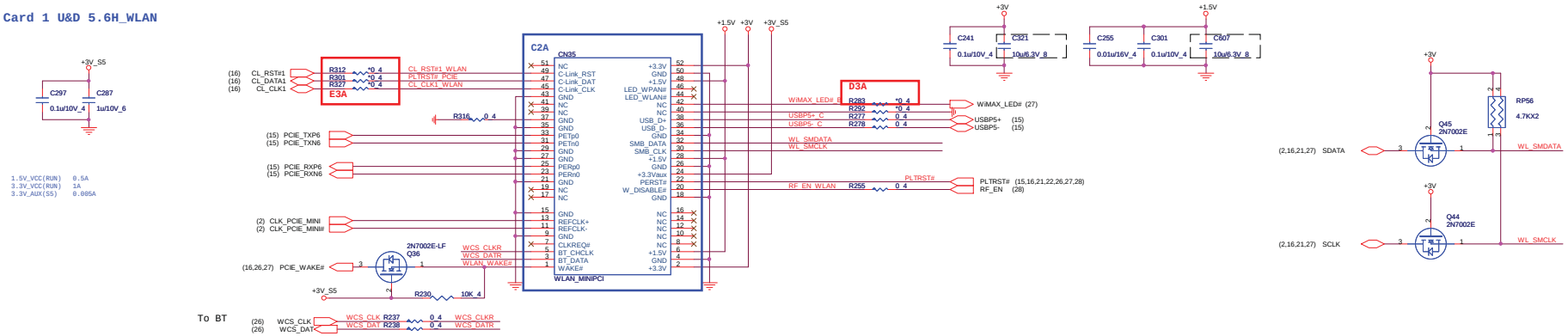


Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	OZ129T(5in1/1394)	1A

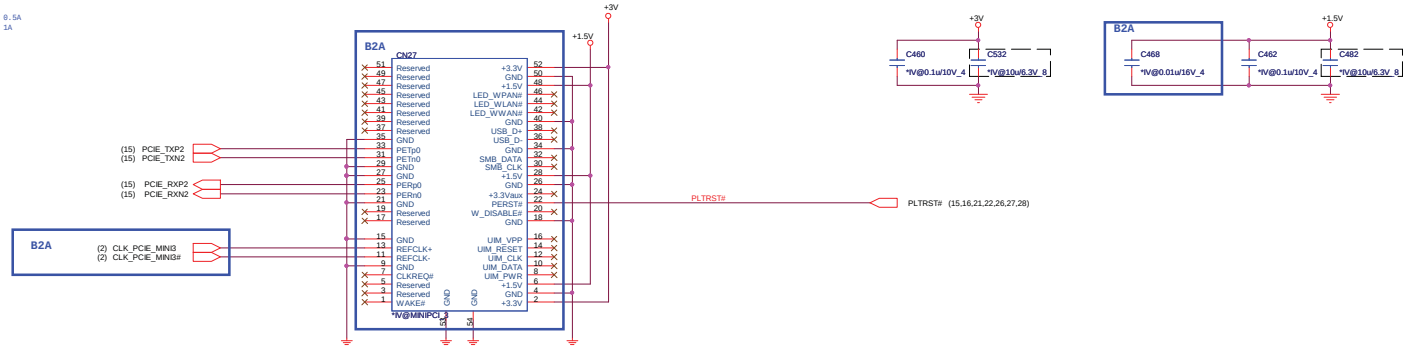
Date: Friday, February 01, 2008 Sheet 24 of 41

MINI Card 1 U&D 5.6H_WLAN



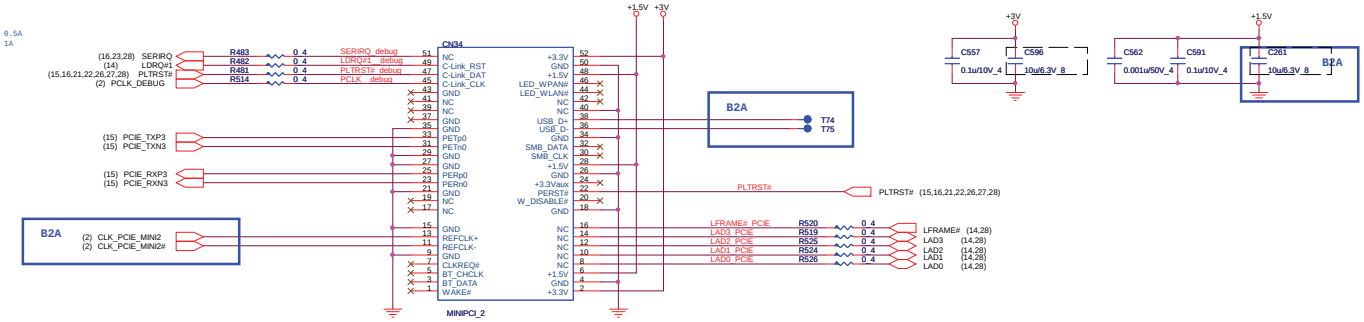
MINI Card 3 U 9H_HD-DVD

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A

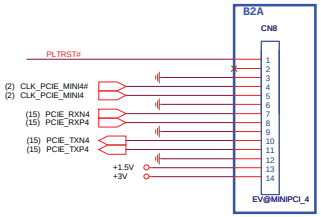


MINI Card 2
U 5.6H_ROBOSON
D 7.5H_HD-DVD

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A



MINI Card 4-D/Robson

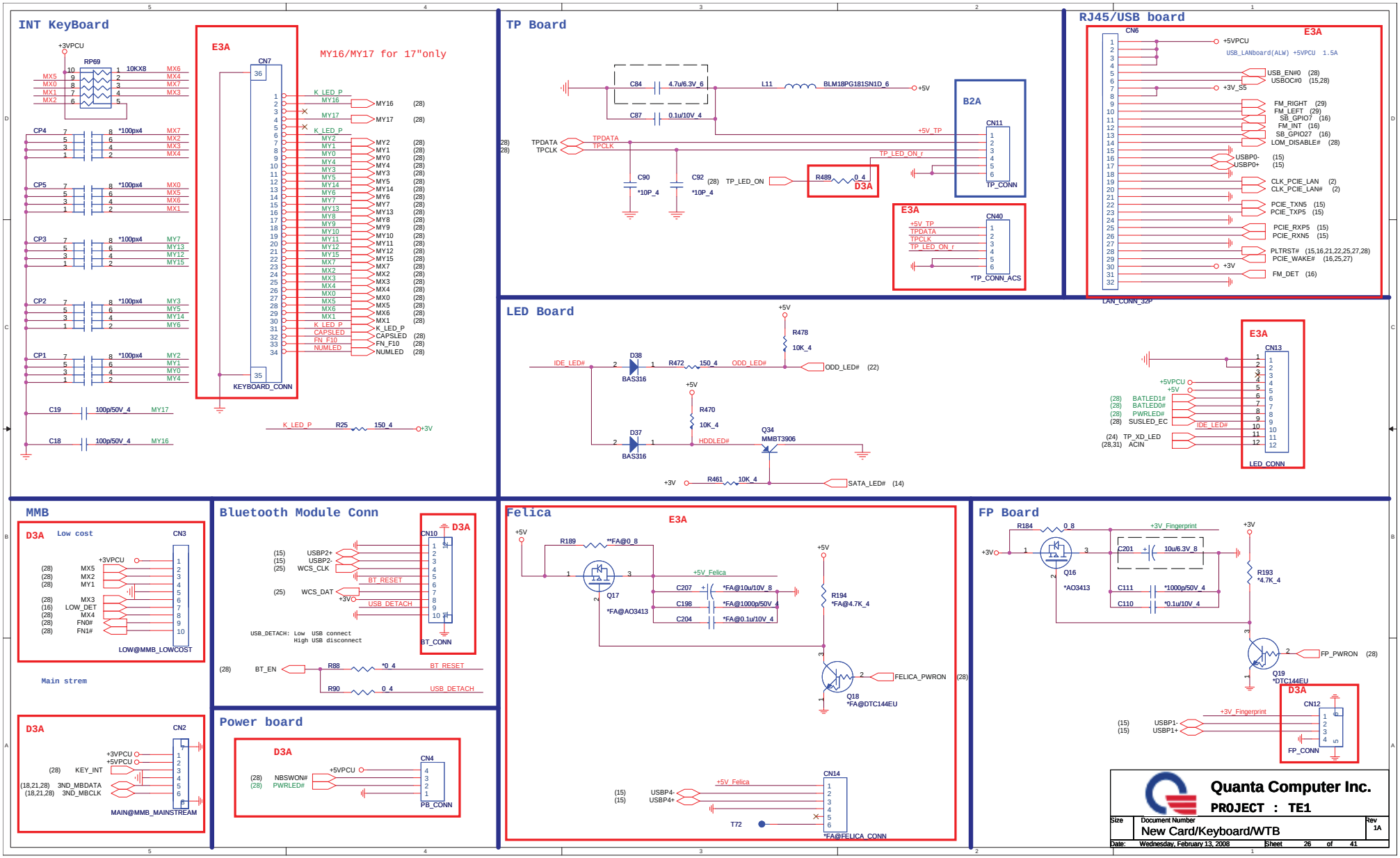


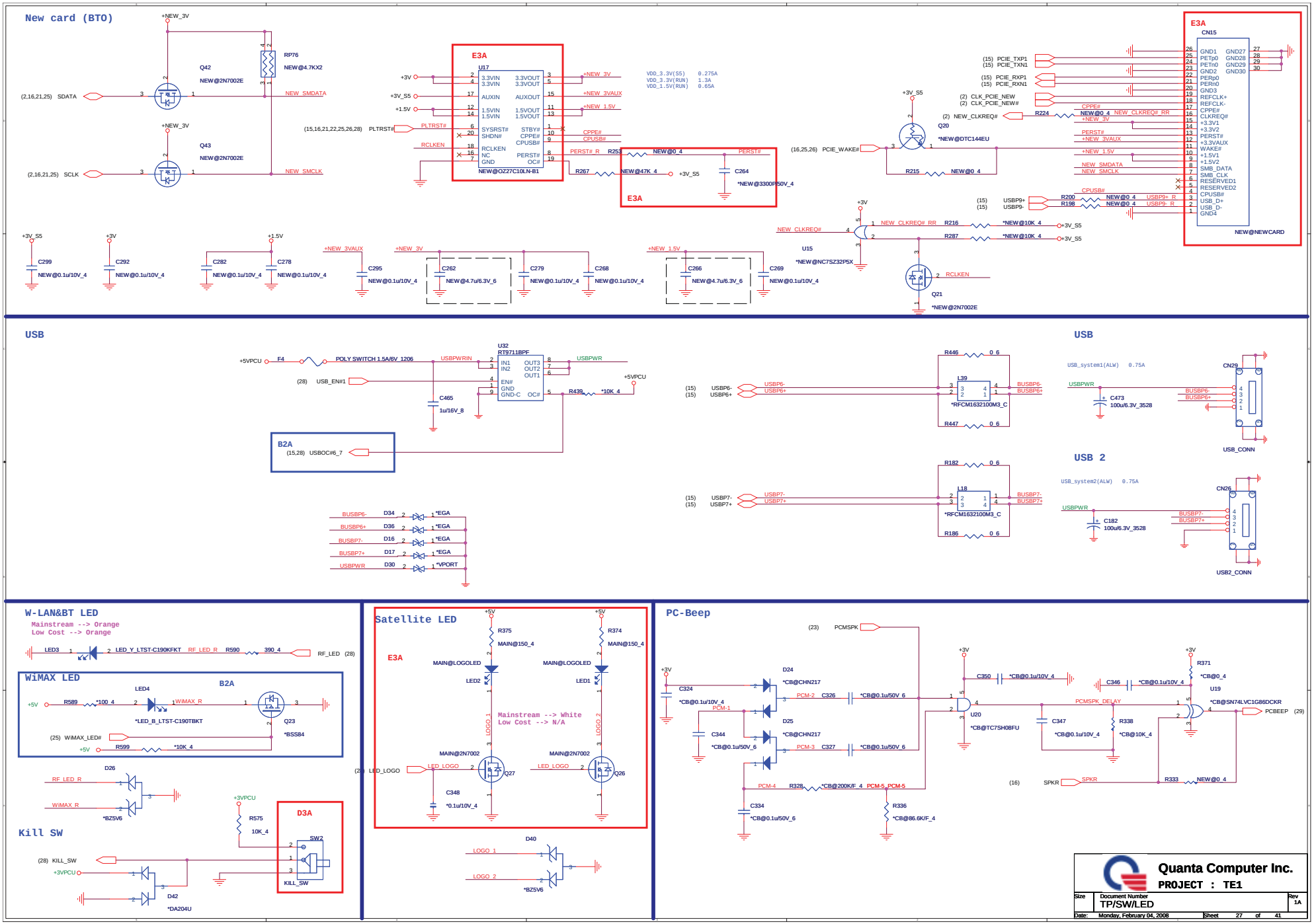
Remark1:TV+Robson or HD-DVD+Robson or TV+HD-DVD for UMA SKU

Remark2:TV is just for UMA(13")

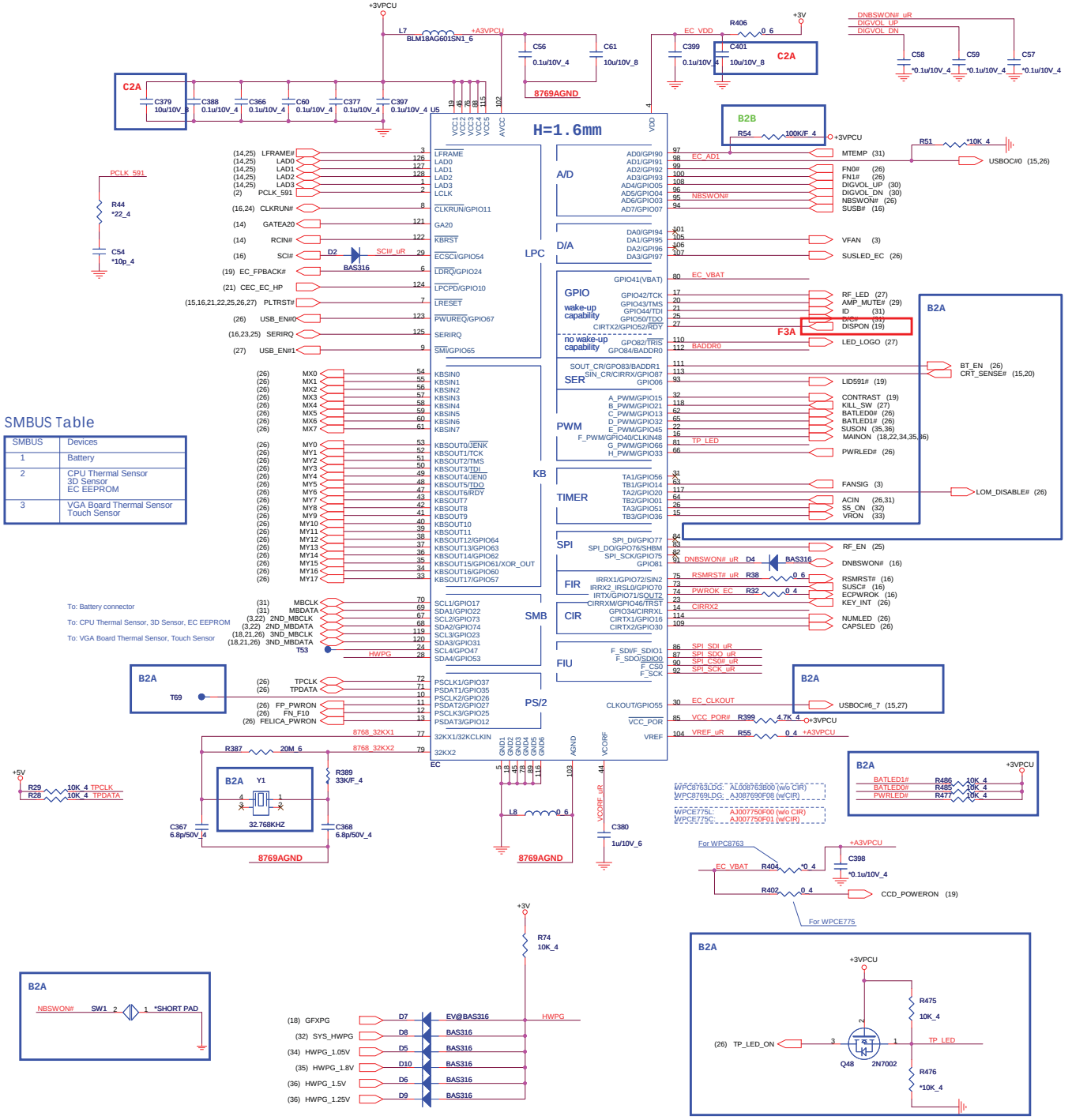
	UMA	Discrete
1	WLAN	WLAN
2	Robson	HD-DVD
3	HD-DVD or Robson	N.C
4	N.C	Robson

Quanta Computer Inc.
PROJECT : TE1
Size: Document Number: MINI CARD Rev: 1A
Date: Thursday, January 31, 2008 Sheet 25 of 41

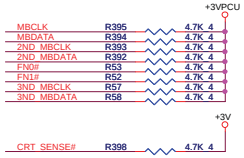

INT KeyBoard
E3A
MY16/MY17 for 17"only
CN7
KEYBOARD_CONN
RP69
10KX8
CP4
CP5
CP3
CP2
CP1
*100px4
C19
100p/50V_4
C18
TP Board
B2A
CN11
TP_CONN
D3A
R489
0_4
C84
4.7u/6.3V_6
L11
BLM18PG181SN1D_6
C87
0.1u/10V_4
C90
*10P_4
C92
TP_LED_ON
E3A
CN40
*TP_CONN_ACS
RJ45/USB board
CN6
LAN_CONN_32P
LED Board
R478
10K_4
R472
150_4
D38
BAS316
R470
D37
Q34
MMBT3906
R461
SATA_LED# (14)
CN13
LED_CONN
MMB
Low cost
CN3
LOW@MMB_LOWCOST
Main strem
CN2
MAIN@MMB_MAINSTREAM
Bluetooth Module Conn
CN10
BT_CONN
USB_DETACH: Low USB connect
High USB disconnect
R88
R90
Power board
CN4
PB_CONN
Felica
R189
**FA@0_8
Q17
*FA@AO3413
C207
*FA@10u/10V_8
C198
*FA@1000p/50V_4
C204
*FA@0.1u/10V_4
R194
*FA@4.7K_4
Q18
*FA@DTC144EU
CN14
T72
*FA@FELICA_CONN
FP Board
R184
0_8
Q16
*AO3413
C201
10u/6.3V_8
C111
*1000p/50V_4
C110
*0.1u/10V_4
R193
*4.7K_4
Q19
*DTC144EU
CN12
FP_CONN
Quanta Computer Inc.
PROJECT : TE1
Size
Document Number
New Card/Keyboard/WTB
Rev
1A
Date: Wednesday, February 13, 2008
Sheet 26 of 41


New card (BTO)
E3A
USB
USB 2
W-LAN&BT LED
Mainstream --> Orange
Low Cost --> Orange
WiMAX LED
Kill SW
Satellite LED
Mainstream --> White
Low Cost --> N/A
PC-Beep
Quanta Computer Inc.
PROJECT : TE1
TP/SW/LED
Monday, February 04, 2008

EC



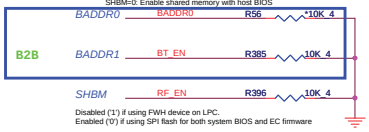
SM BUS PU



I/O Base Address

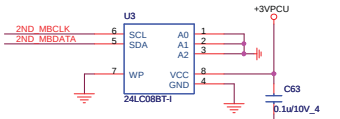
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS



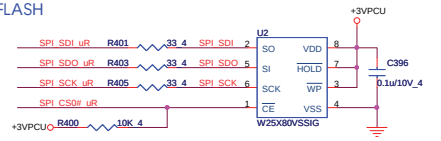
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID



ADDRESS: A0H

SPI FLASH

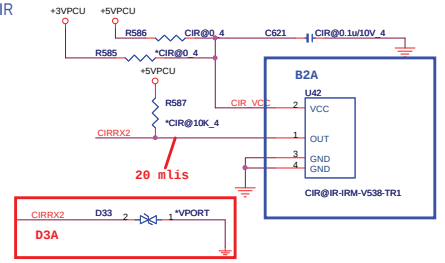


2nd sorce

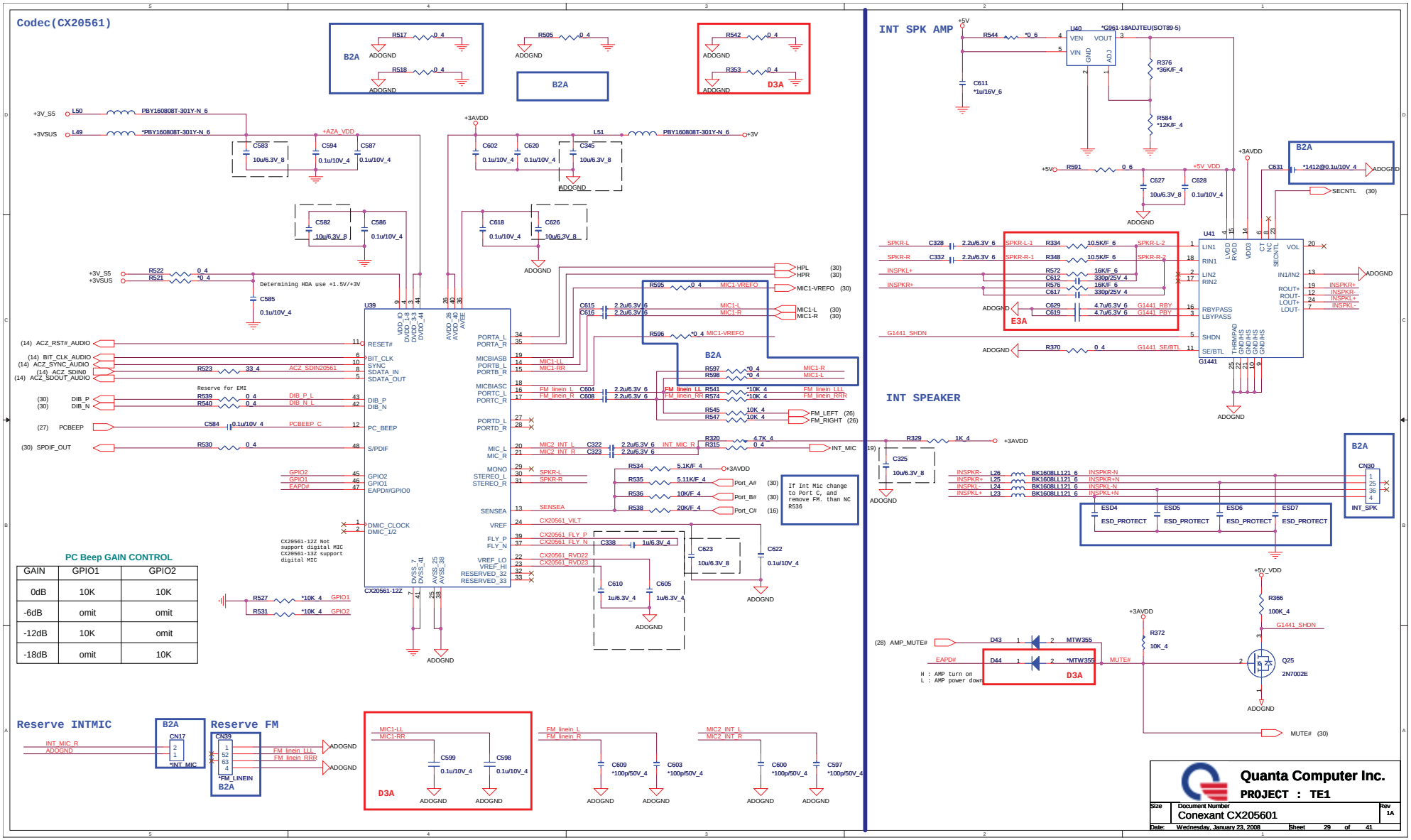
MXIC	MX25L8005M2C-15G	AKE5GFK0Z09
Winbond	W25X80VSSIG	AKE3GFP0N08
EON	EN25F80-75HCP	AKE3GZP0Q00

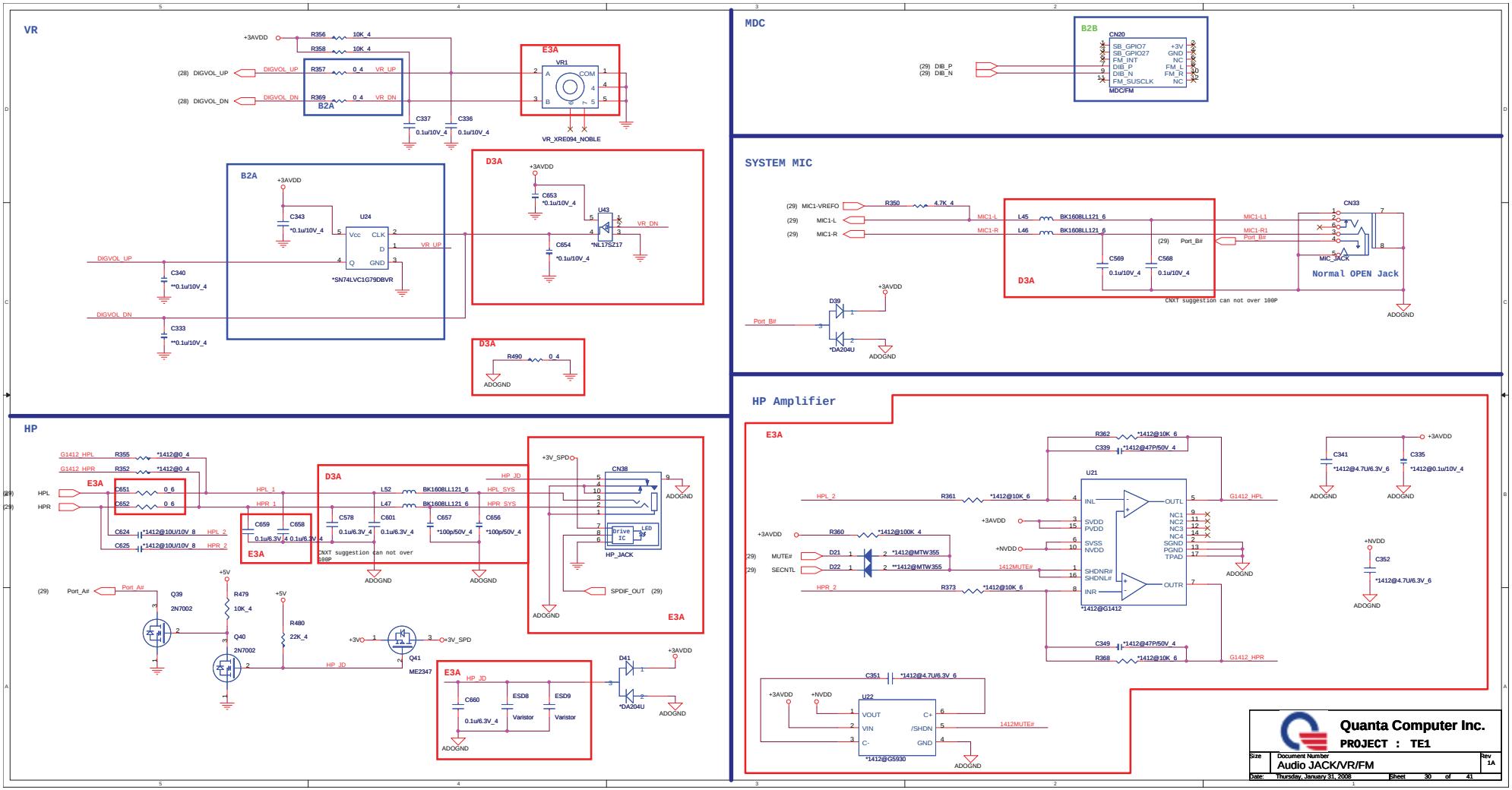
INTERNAL KEYBOARD STRIP SET

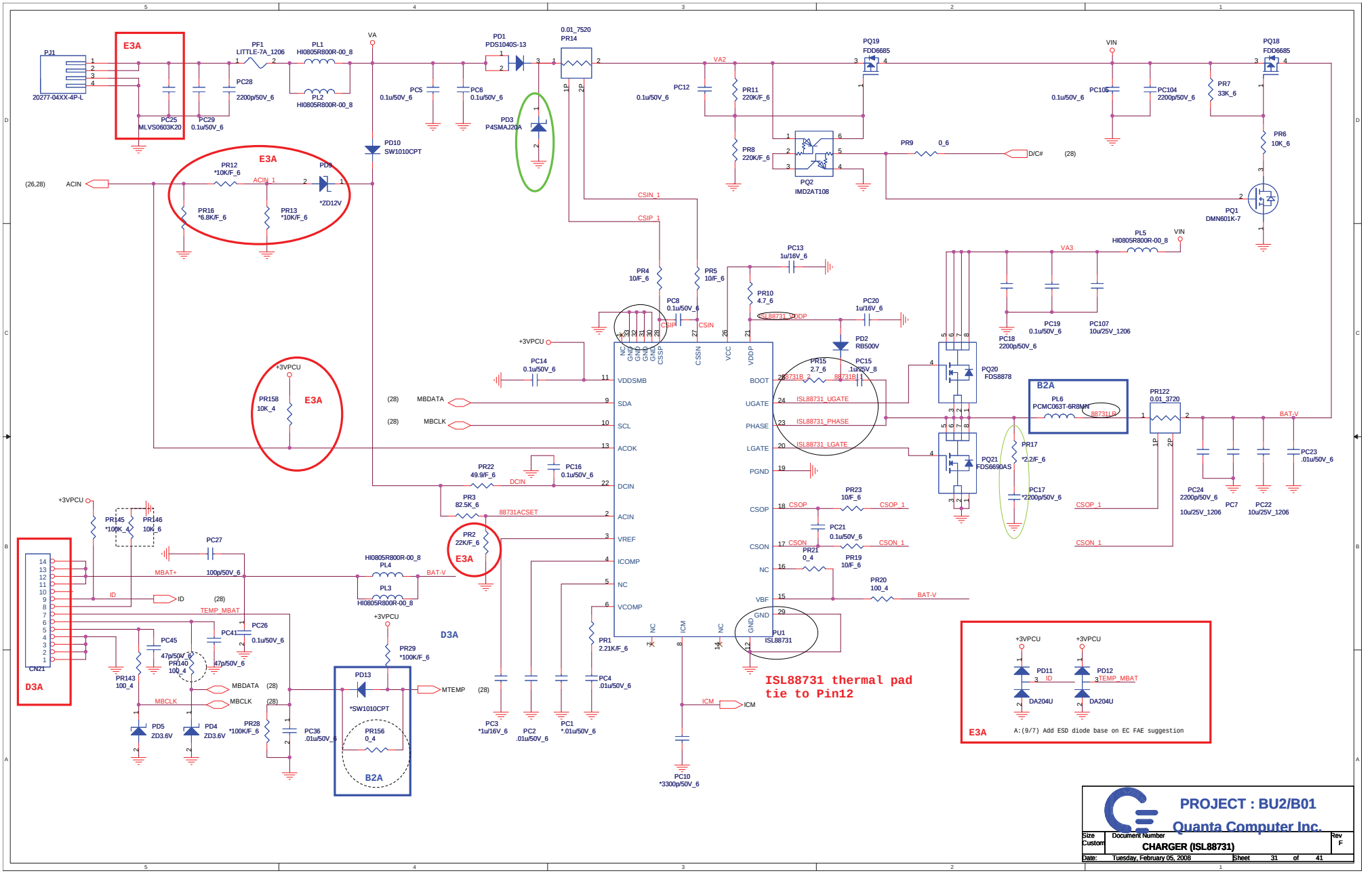
CIR

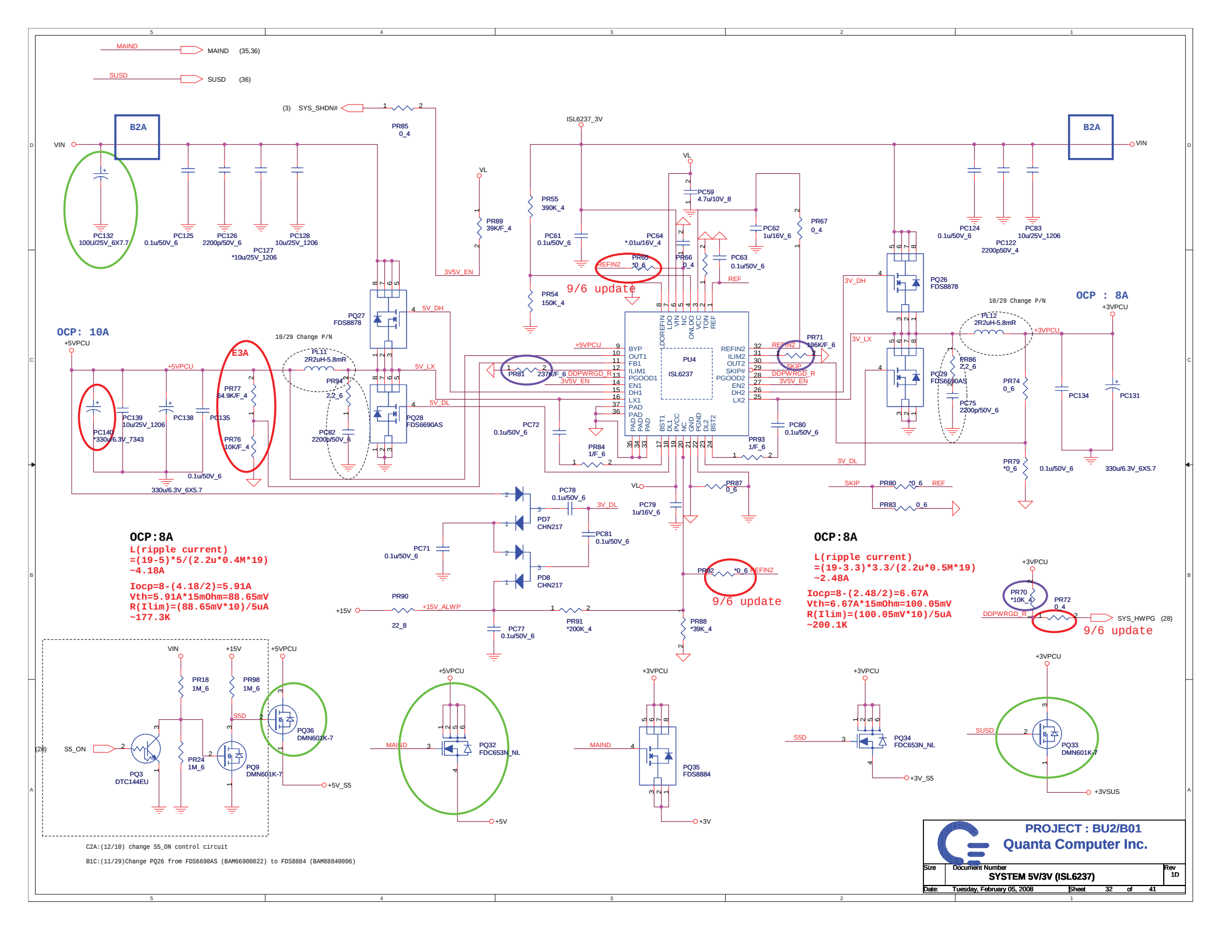


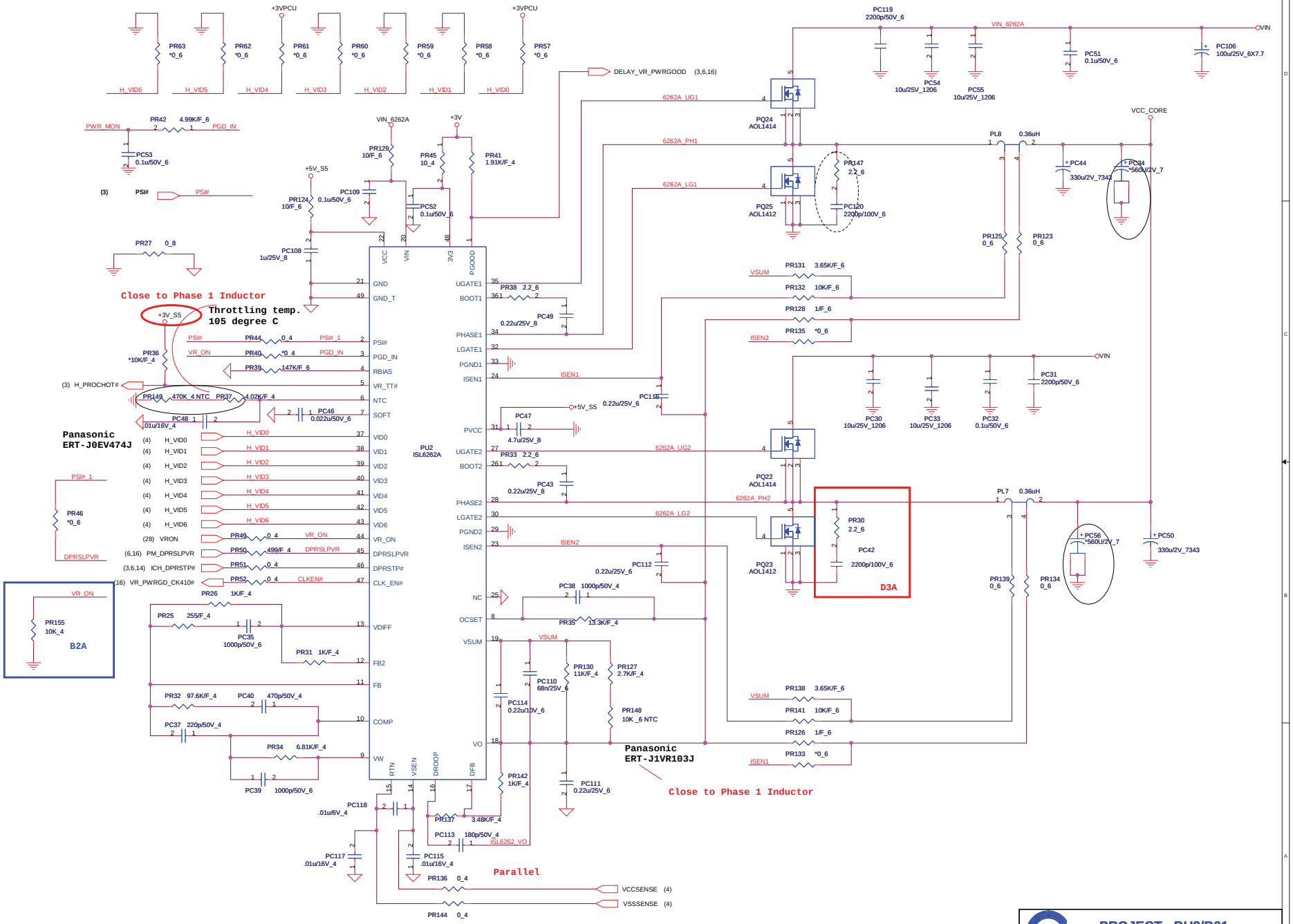
Quanta Computer Inc.
PROJECT : BU1
Size | Document Number EC-PC8763 | Rev 3A
Date: Tuesday, February 05, 2008 | Sheet 28 of 41


Codec(CX20561)
INT SPK AMP
INT SPEAKER
Reserve INTMIC
Reserve FM
PC Beep GAIN CONTROL
GAIN | GPIO1 | GPIO2
0dB | 10K | 10K
-6dB | omit | omit
-12dB | 10K | omit
-18dB | omit | 10K
CX20561-12Z
U39
U40
U41
G1441
E3A
D3A
B2A
Quanta Computer Inc.
PROJECT : TE1
Conexant CX205601
Rev 1A
Wednesday, January 23, 2008
Sheet 29 of 41


VR
MDC
SYSTEM MIC
HP
HP Amplifier
Normal OPEN Jack
Quanta Computer Inc.
PROJECT : TE1
Audio JACK/VR/FM
Thursday, January 31, 2008


E3A
PJ1
20277-04XX-4P-L
PF1
LITTLE-7A_1206
PL1
HI0805R800R-00_8
PL2
HI0805R800R-00_8
PC25
MLVS0603K20
PC28
2200p/50V_6
PC29
0.1u/50V_6
VA
PD1
PDS1040S-13
0.01_7520
PR14
PC5
0.1u/50V_6
PC6
0.1u/50V_6
PD3
P4SMAJ20A
PD10
SW1010CPT
PQ19
FDD6685
VA2
PC12
0.1u/50V_6
PR11
220K/F_6
PR8
220K/F_6
PQ2
IMD2AT108
PR9
0_6
D/C#
(28)
VIN
PC105
0.1u/50V_6
PC104
2200p/50V_6
PR7
33K_6
PQ18
FDD6685
PR6
10K_6
PQ1
DMN601K-7
(26,28)
ACIN
PR12
*10K/F_6
ACIN_1
PD9
*ZD12V
PR16
*6.8K/F_6
PR13
*10K/F_6
CSIN_1
CSIP_1
PR4
10/F_6
PR5
10/F_6
PC13
1u/16V_6
PC8
0.1u/50V_6
PR10
4.7_6
ISL88731_VDDP
PC20
1u/16V_6
PD2
RB500V
PC14
0.1u/50V_6
+3VPCU
PR158
10K_4
(28)
MBDATA
MBCLK
ACOK
PR22
49.9/F_6
DCIN
PC16
0.1u/50V_6
PR3
82.5K_6
88731ACSET
PR2
22K/F_6
VA3
PL5
HI0805R800R-00_8
PC19
0.1u/50V_6
PC107
10u/25V_1206
PC18
2200p/50V_6
PR15
2.7_6
88731B
PC15
.1u/25V_8
PQ20
FDS8878
B2A
PL6
PCMC063T-6R8MN
PR122
0.01_3720
BAT-V
PC23
.01u/50V_6
PC24
2200p/50V_6
PC7
10u/25V_1206
PC22
10u/25V_1206
PR17
*2.2/F_6
PC17
*2200p/50V_6
PQ21
FDS6690AS
CSOP_1
CSON_1
PR145
*100K_4
PR146
10K_6
PC27
100p/50V_6
MBAT+
ID
TEMP_MBAT
CN21
D3A
PC45
47p/50V_6
PR140
100_4
PC41
47p/50V_6
PC26
0.1u/50V_6
PR143
100_4
MBDATA
MBCLK
PD5
ZD3.6V
PD4
ZD3.6V
PR28
*100K/F_6
PC36
.01u/50V_6
HI0805R800R-00_8
PL4
PL3
HI0805R800R-00_8
BAT-V
PR29
*100K/F_6
PD13
*SW1010CPT
MTEMP
PR156
0_4
B2A
D3A
PR23
10/F_6
PC21
0.1u/50V_6
PR21
0_4
PR19
10/F_6
PR20
100_4
PR1
2.21K/F_6
PC4
.01u/50V_6
PC3
*1u/16V_6
PC2
.01u/50V_6
PC1
*.01u/50V_6
PC10
*3300p/50V_6
ICM
PU1
ISL88731
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731 thermal pad
tie to Pin12
PD11
PD12
DA204U
ID
TEMP_MBAT
A:(9/7) Add ESD diode base on EC FAE suggestion
PROJECT : BU2/B01
Quanta Computer Inc.
CHARGER (ISL88731)
Size
Custom
Document Number
Rev
F
Date:
Tuesday, February 05, 2008
Sheet
31
of
41


MAIND
MAIND (35,36)
SUSD
SUSD (36)
(3) SYS_SHDN#
PR85 0_4
B2A
VIN
PC132 100U/25V_6X7.7
PC125 0.1u/50V_6
PC126 2200p/50V_6
PC127 *10u/25V_1206
PC128 10u/25V_1206
ISL6237_3V
VL
PR89 39K/F_4
3V5V_EN
PR55 390K_4
PC61 0.1u/50V_6
PC64 *.01u/16V_4
PR65 *0_6
PR66 0_4
PC59 4.7u/10V_8
PC62 1u/16V_6
PR67 0_4
PC63 0.1u/50V_6
REF
REFIN2
PR54 150K_4
9/6 update
PC124 0.1u/50V_6
PC122 2200p50V_4
PC83 10u/25V_1206
B2A
VIN
OCP: 10A
+5VPCU
E3A
10/29 Change P/N
PL11 2R2uH-5.8mR
PR94 2_2_6
PC82 2200p/50V_6
PR77 64.9K/F_4
PR76 10K/F_4
PC140 *330u/6.3V_7343
PC139 10u/25V_1206
PC138
PC135
0.1u/50V_6
330u/6.3V_6X5.7
PQ27 FDS8878
PQ28 FDS6690AS
5V_DH
5V_LX
5V_DL
PU4 ISL6237
PR81 237K/F_6
DDPWRGD_R
PC72 0.1u/50V_6
PR84 1/F_6
PR93 1/F_6
PC80 0.1u/50V_6
PR71 196K/F_6
PQ26 FDS8878
PQ29 FDS6690AS
3V_DH
3V_LX
3V_DL
SKIP
PR80 *0_6
PR83 0_6
PR86 2_2_6
PC75 2200p/50V_6
PR74 0_6
PR79 *0_6
PC134
PC131
330u/6.3V_6X5.7
OCP : 8A
10/29 Change P/N
PL12 2R2uH-5.8mR
+3VPCU
PC78 0.1u/50V_6
PC79 1u/16V_6
PR87 0_6
PD7 CHN217
PD8 CHN217
PC81 0.1u/50V_6
PC71 0.1u/50V_6
PR90 22_8
+15V_ALWP
PR91 *200K_4
PC77 0.1u/50V_6
PR88 *39K_4
PR92 *0_6
9/6 update
OCP:8A
L(ripple current) =(19-5)*5/(2.2u*0.4M*19) ~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=5.91A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA ~177.3K
OCP:8A
L(ripple current) =(19-3.3)*3.3/(2.2u*0.5M*19) ~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA ~200.1K
PR70 *10K_4
PR72 0_4
SYS_HWPG (28)
9/6 update
+15V
PR18 1M_6
PR98 1M_6
PR24 1M_6
S5D
S5_ON
(28)
PQ3 DTC144EU
PQ9 DMN601K-7
PQ36 DMN601K-7
+5V_S5
PQ32 FDC653N_NL
+5V
PQ35 FDS8884
+3V
PQ34 FDC653N_NL
+3V_S5
PQ33 DMN601K-7
+3VSUS
C2A:(12/10) change S5_ON control circuit
B1C:(11/29)Change PQ26 from FDS6690AS (BAM66900022) to FDS8884 (BAM88840006)
PROJECT : BU2/B01
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1D
Date: Tuesday, February 05, 2008
Sheet 32 of 41

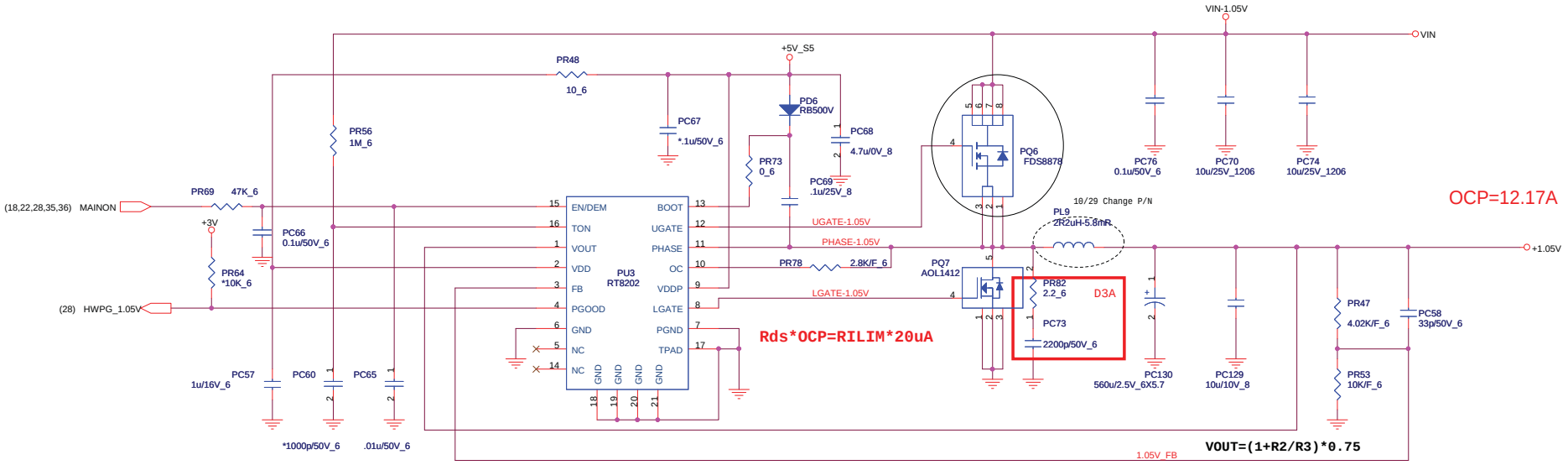


PROJECT : BU2/B01

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU CORE(ISL6262A)	F

Date: Wednesday, January 23, 2008 Sheet 33 of 41



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

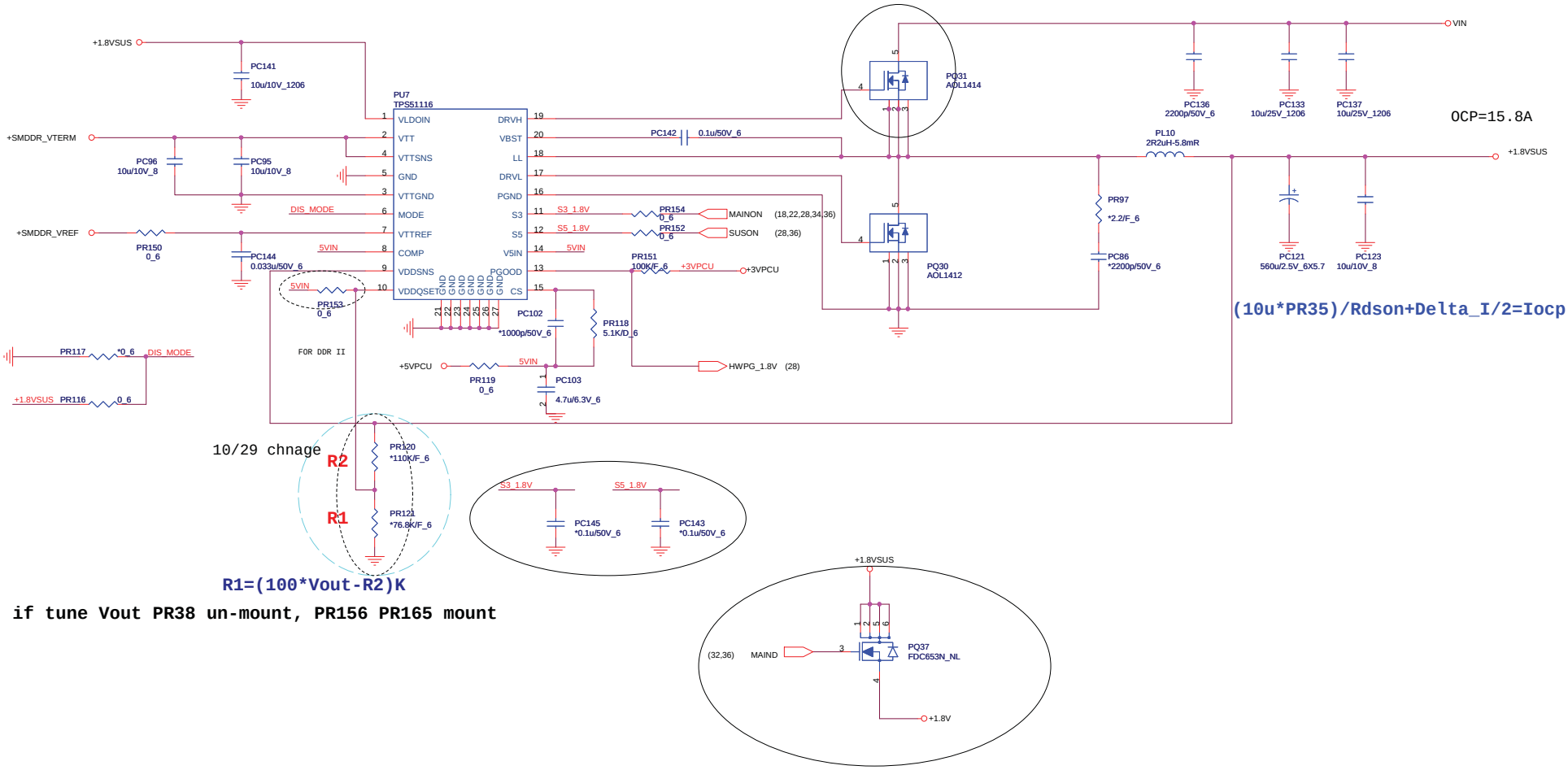
AO1412 Rds=4.6mOhm

12.17A OCP --- OC=2.8K(CS22803F914)

PROJECT : BU2/B01

Quanta Computer Inc.

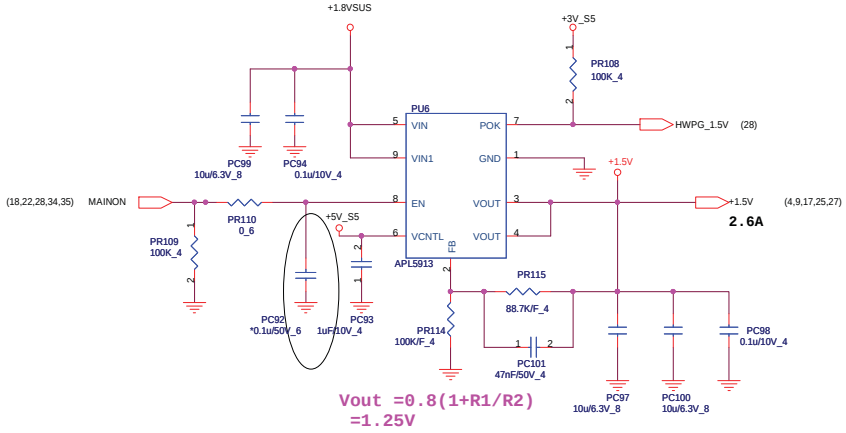
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1D
Date: Wednesday, January 23, 2008	Sheet 34 of 41	

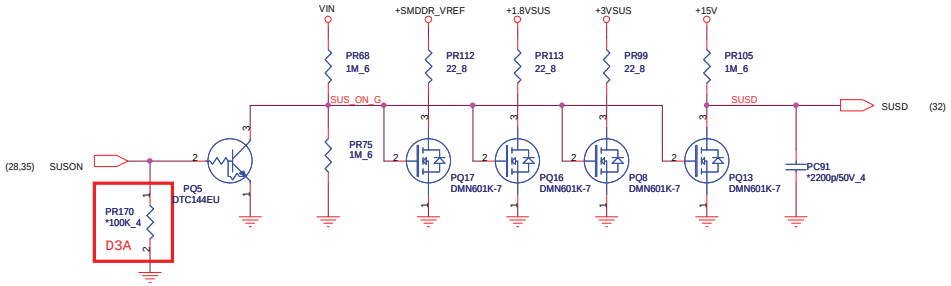


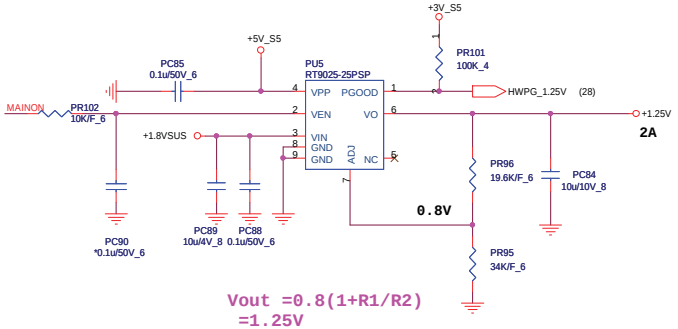
PROJECT : BU2/B01

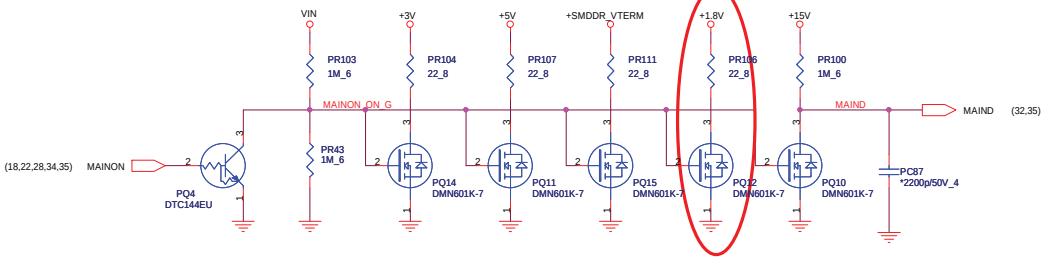
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	F
Date: Wednesday, January 23, 2008	Sheet 35 of 41	









PROJECT : BU2/B01

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	F
Date: Wednesday, January 23, 2008	Sheet 36 of 41	

Model	REV	DATE	CHANGE LIST	NOTE
TE1	01	20070824	FIRST RELEASED : 20070824	
	A1A	20070927	FIRST RELEASED : 20070927	
	B2A		Page 22 : U31 for G-sensor SKU must stuff,and add GS@ for BOM clear.	
			Page 22 : Change Y4/C476/C485 Value from * to **,because Gensor function default not need that.	
			Page 3/14 : Q6/Q9/Q33 BA039040039 change to BA0390400H0 for before BA039040039 cause RTC charger issue	
			Page 28 : Change SW1 to short PAD for debug only	
			Page 19 : For LED Panel C9/R10 always reserve	
			Page 14/28 : Y1/Y6 shortage issue change from BG332768909 to BG332768224	
			Page 3 : R81 stuff 10K for OD pin	
			Page 31 : CN21 BOM error,change DFHD07MR000 to DFHD14MS011	
			Page 17 : C540/C606/C289 CH6102ME904(EOL) change to CH6102M1909	
			Page 22 : U34 G-sensor P/N change same as BU1 from AL021174C00 to AR0BU1R0000	
			Page 21 : ESD1/ESD2/ESD3 always reserve for ESD solution.Change value to **	
			Page 18 : CN31/R471/R459/C530/C531/C553/C552/C486/R453/R457/R452/R458 add EV@	
			Page 27 : CN15(New card) change PCB Footprint to "ncard-13180151-u-26p-l "	
			Page 27 : U17 Value change from NEW@OZ27C10LN-B1 to NEW@OZ27C10LN-C1.Let P/N and Value match.	
			Page 21 : U11 P/N error. so change to "new part number" avoid before use error BOM.U11 reserve for sil1392.	
			Page 21 : U12 Value add IHM@ fo BOM clear.To avoid BOM build error.	
			Page 21 : U9 Value must modify from *CEC@R5F211A4SP to CEC@R5F211A4SP.To clear BOM.	
			Page 25 : CN27/CN34 MINI Card clock connect error.CN27 must connect to CLK_PCIE_MINI3/3#.CN34 must connect to CLK_PCIE_MINI2/2#.	
			Page 24/25 : C261/C246 must stuff.Before NC for A-test layout issue only.	
			Page3 : RP45 Value add NEW@ for new card clock BOM clear and better EMI result.	
			Page2 : R226 Value add *CB@ for PCMCIA clock BOM clear and better EMI result.	
			Page31 : PL6 Change PCB Footprint to "CHOKE-PCMC063T-3R3MN-BD3A" for SMT issue.	
			Page19 : U1 add pin27 to GND to meet PCB Footprint.	
			Page20 : U25 Pin3/Pin5 SWAP for layout smooth	
			Page30 : Del FM interface,Move to LAN/B.and Del C400.	
			Page26 : LAN/B CONN change to 30pin(BL121-30R-30P-L-TE1,DFFC30FR009),and add FM interface	
			Page22 : C31 change Footprint from 7343 to 3528 for placement no space for EC X'tal move.	
			Page26 : CN13 Change Footprint to 88060-12001-12P-L for ME assembly issue.	
			Page28 : U42(CIR) Change PCB Footprint for SMT suggestion,And change P/N from BEBK0076Z00 to BEBK0038Z00	
			Page29/30 : HP AMP NC,Reserve only.	
			Page26 : Del R103, TP(Mainstrem/low cost control by TP/B)	
			Page15/27 : Add R592/R593 for USB port match OC port	
			Page21 : Add R103/R594/Q46/Q47/R600/R601 for CEC level shift(BOI mail).And adjust net name for ESD protect ESD1 close to connector.	
			Page29 : Reserve R595~R598 for Audio WHQL issue.(Can not mulite strem when FM not support.	
			Page27 : LED1/LED2 change type for ME.And modify LED4 Wimax LED circuit	
			Page20 : HOLE 16 add GND for ESD	
			Page21 : Del D13/R115/R116/D14 same as BL5S	
			Page28 : EC del MMB(10pin)LED0#/1#/2#.And move BT_EN/CRT_SENSE#	
			Page26 : CN2 modify Footprint to BL123-06R-6P-L-BL5,P/N to DFFC06FR336	
			Page26 : CN4 modify Footprint to BL123-04R-4P-L-BL5,P/N to DFFC04FR012.And SWAP pin list for different Footprint	
			Page26 : CN11/CN14 modify Footprint to BL121-06R-6P-L-BL5,P/N to DFFC06FR003.	
			Page25 : CN8 modify Footprint to BL123-14R-14P-L-TE1,P/N to DFFC14FR009.	
			Page22 : CN19 change HDD Footprint to SATA-070820-QU001-22P-R-TE1	
			Page2 : C231/C234 for Y3 TXC measurement suggestion change from 33p to 30p	
			Page24 : C580/C575 for Y3 TXC measurement suggestion change from 10p to 15p	
			Page20 : Del HOLE3 for ME request	
			Page26/28 : Add LOM_DISABLE# for LAN power consumption	
			Page2 : Change R214/R211 from 33ohm to 47ohm for EA fail.	
			Page29 : CN30 use same parts for BOI project. Change to SCY DFWF04MS002.	
			Page20 : HOLE14/HOLE18 modify footprint for new card move 2mm for BOI request.	
			Page27 : Kill switch(SW2) change part for ME request.P/N is DHLLSS12P07	
			Page14 : RTC Circuit R455/R456/R449/R450 follow standar circuit value(Eric Lee)	
			Page13 : CN24 Chnage Footprint from DDR-C-292564-200P to DDR-C-292564-200P-TE1 for connector fixed pad not meet Footprint.	
			Page15/25 : Not support TV,Del USB8 and add T71/T73/T74/T75	
			Page24 : C542 stuff 22p for EMI issue.	
			Page29 : Add R517/R518 0 ohm for EMI issue.	
			Page20 : +5V/VIN add 0.1u to shape for EMI issue	
			Page17 : SB CAP cost down C579/C267	
			Page8/9 : NB CAP cost down C118/C458/C69/C155/C403/C149/C443/C436	
			Page2 : CLK CAP cost down C541	
			Page24 : Card reader cost down,del 0 ohm	
			Page19 : C16 change BOM/Footprint from CH6101M9905 to CH61001ME96 for cost down	
			Page27 : C262/C266/C84 change BOM/Footprint from CH5472K9A02 to CH5471M9907 for cost down	

Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	Change list	1A

Date: Saturday, January 19, 2008 Sheet 37 of 41

Model	REV	DATE	CHANGE LIST	NOTE
TE1	B2A		Page2429 : C567/C338/C610/C605 change BOM from CH5102K9B06 to CH5101K9B01 for cost down	
			Page?? : C596/C261/C607/C321/C482/C532/C201/C583/C582/C345/C626/C325/C623/C360/C24/C281 change BOM from CH6102K9A01 to CH61001ME96 for cost down	
			Page4 : CPU CAP C35 BOM change for cost down from CH733LM8812 to CH733RM8858	
			Page9/17 : C293/C254/C283/C102 cost down from CH5472M9901 to CH5471M9907	
			Page19 : C27 change BOM/Footprint from CH61004M398 to CH61004M291 for cost down	
			Page16 : Add FM_Detect pin to GPIO12	
			Page3 : Del C50,Add R115/R116 for shut down circuit	
			Page16 : Add FM_Detect pin to GPIO12	
			Page20 : HOLE11/HOLE28 modify Footprint for ME issue	
			Page29 : Del R528 for no space adjust modem trace	
			Page32 : Del JP1/JP2	
			Page19 : Reserve R473/R474 200K for LED drive IC	
			Page33 : Add PR155 for VRON stable	
			Page31 : MTEMP add PD13/PR156	
			Page21 : CN23(HDMI) Connect chnge Footprint and library pin define for correct library from HDMI-C12815-119A5-L-19P-V to HDMI-C12815-119A5-L-19P-V-TE1	
			Page26 : CN6 apply pin 31 and pin32. modify new footprint : BL121-32R-32P-L-TE1	
			Page29 : Change C224, C226, C227 and C228 to ESD PROTECT (ESD4, ESD5, ESD6 and ESD7 : DIODE SMD V-PORT-0603-220K-V05)	
			Page20 : C650 change to 1000P from EMI request	
			Page28 : Apply isolate TP_LED_ON from EC to Mainstream TP	
			Page20 : C641 ~ C649 apply to CC0402 = CH4104K9B03	
			Page31-38 : Update power circuit to TE1_965PM_B2A-1030-1030	
			Page20 : L1-L3 change to CX8LL470000 from EMI suggestion	
			Page20 : Modify Hole26, NC GND net for layout issue	
			Page21 : *IHM@1000p/16V_4 change to *IHM@1000p/50V_4	
			Page25 : C468 change Value from 0.01u/25V_4 to 0.01u/16V_4	
			Page25 : CN27 change to DFHD52MS146	
			Page19, 29 : INT_MIC change PN to DFHD02MR003	
			Page29 : CN39 change to DFHD04MR012	
			Page26 : CN13 change to DFFC12FR006	
			Page14 : CN28 change to DFWF02MS000	
			Page29 : R351, R354 change footprint to RC0603	
			Page26 : modify Low cost MMB pin define, CN3 pin2 change to MX5	
			Page28 : apply R486, R485 and R477 PU for Battery LED issue follow BL5	
			Page15 : Del T73, T71 for layout isse (use via to measure)	
			Page20 : del Hole10 and Hole 27 GND pin (layout issue)	
			Page30 : Stuff R357 and R369, reserve C343 U24 R367 Q24 for VR smooth modify	
			Page21 : R144 Value add /F	
	B2B		Page21 : Q7/Q8 Value add CEC@ for BOM option	
			Page21 : F3 Value add IEHM@ for BOM option	
			Page4 : C40/C41 stuff for power measurement issue	
			Page28/31 : PR29 NC / R54 stuff 100K/F for S.Y request	
			Page30 : R516/R543 stuff 1K / R354/R351 stuff 10u/10v_6	
			Page30 : VR1 change P/N from CK0000RZ004 to CK0000RZ005	
			Page15 : R569 Value add EV@ for BOM option	
			Page14 : R300/R330/R561/R562 Value add *IHM for BOM option	
			Page19 : C13 change to 33n / R14 change to 499/F. and reserve R473 and R474	
			Page- : C289, C540, C606, R351, R354 change to CH6101M9905 for Buyer issue	
			Page16 : Stuff R248 and change 0_4, and Stuff C242 change to 10p_4 for CLKUSB_48 EA fail issue	
			Page30 : CN20 change PN to DFHS12FS000 with SUY forbidden issue	
			Page28 : Add R385 and NC R56 for Boardcom BT issue	
	C2A		Page04 : C40 change Value to PC146. C41 change to PC147	
			Page30 : R354 change Value to C651. R351 change to C652.	
			Page31 : Mirror CN21 Pin define	
			Page25 : CN35 change footprint:MIPCI-88958-5204M-52P-H	
			Page28 : C379 and C401 change PN to CH6102K9A19 with BOI issue	
			Page25 : CN35 change to DIP type (footprint:MIPCI-88958-5204M-52P-V), Part Number (DFHS52FR013)	
			Page24 : CN37 change footprint to (4IN1-CM4R-118-43P-L-V), Part Number (DFHD42MS005)	

Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	Change list	1A

Date: Saturday, January 19, 2008 Sheet 38 of 41

Model	REV	DATE	CHANGE LIST	NOTE
TE1	D3A		Page19 : modify MR seneor with BLON circuit to solve flashing issue when system shut-down	
			Page30 : Change Q24 to U43 to solve VR not smooth	
			Page31,32 : Change Charger circuit to use ACOK to inform EC	
			Page29 : NC D44 to solve switch mute to un-mute, sound will delay about 2seconds	
			Page24 : Apply R351, R354, R367, R487 and R488 for EMI request	
			Page20 : EMI suggest used LL680 + 4.7 pf x6 cap to avoide CRT issue	
			Page19 : Apply U44 circuit for LED panel black light issue	
			Page27 : Change LED1 and LED2 to new part	
			Page3,5 : Apply L54 near CPU side and C666 near NB side for ESD issue	
			Page36 : Reserve SUSON PD resistor	
			Page28 : Apply R489 reserve for TP_LED_ON enable(Low Cost ID)	
			Page03 : NC C71 for Fansing speed issue follow BL5S	
			Page-- : Logo LED, function board conn and Board ID Value apply function option	
			Page21 : HDMI conn change footprint to HDMI-C12815-119A5-L-19P-V-BU2	
			Page25 : Led board conn change PN and Footprint : DFFC12FR285	
			Page25 : Function board conn (mainstream and lowcost) change PN	
			Page20 : Hole26 change footprint to h-te327x313bc295d98p2-7	
			Page22 : SATA conn change Footprint to SATA-070820-QU001-22P-R-TE1	
			Page-- : DDR socket CN24 change PN to DGMK0000040	
			WLAN minicard conn change PN to DFHS52FR016	
			Battery conn change PN to DFHD14MS014	
			ODD conn change PN to DFHS50FR034	
			1394 conn change PN to DFHS04FR109	
			Kill switch change PN to DHLLSS12P02	
			FP board conn change PN to DFHD04MRA75	
			BT conn change PN to DFHD10MR008	
			CN3 change PN and Footprint is BL136-10R-10P-L	
			CN2 chaneg PN and Footprint is BL136-06R-6P-R	
			Page-- : R275, C307, C308 , R326, R293, R248 change Footprint to -C (circle pad)	
			Page30 : Reserve R490 near VR for ESD portect	
			Page28 : Reserve D33 near CIR for ESD portect	
			Page30 : Reserve C656, C657 for audio noise debug	
			Page21 : NC R136 and C131 to solve HDMI I-diagram fail	
			Page30 : Stuff AMP1412 circut for audio noise test.	
			Page30 : Change L52, L47 to BK1608LL121 and C578 and C601 to 0.1uF to test 3G/GPRS ExpressCard noise in HP.	
			Page29-30 : C599, C598, C569, C568 apply to CH41002KB93, And L45, L46 change to CX8LL121002 for INT MIC recording noise.	
			Page30 : NC R516 and R543 to meet HP Jack signal measure and HP plug- unplug haven't happen bobo-sound too.	
			Page30 : Change C578 and C691 for 0.1u to 0.22u to enhance avoid 3G noise and meet HP Jack signal measure	
			Page25 : 刪Mini card 設計 , MB8~MB11	

Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	Change list	1A

Date: Saturday, January 19, 2008 Sheet 39 of 41

Model	REV	DATE	CHANGE LIST	NOTE
TE1	D3A			
			Inner Document	
			Change C221 to CH01506JBD9, and NC R248, C242 for CLKUSB48 measure pass	
			Add R353 to CS00002JB38 for ESD request	
			Change CN4 PN to DFFC04FR213	
			Add R459 and R471 to CS00002JB38 for EV request	
			Remove Felica function at EV sku	
			Remove MAIN@ parts at Low Cost ID Q26,Q27,R374 and R375	
			Add R542 and R490 for ESD request	
			Change R516, R543, C578 and C601 to CH41002KB93	
	E3A	20080116	Page21 : Change HDMI connector footprint to B test (HDMI-C12815-119A5-L-19P-V-TE1)	
			Page26 : Change CN6 to BL134-32RL-TA1G-32P-L	
			Page20 : Hole26 apply AGND pin for ESD	
			Page30 : HP jack pin9,10 apply GND for ESD	
			Page19,31 : Power modify for LED panel	
			Page26 : Apply CN40 for TP connector 2nd source(ACS)	
			Page21 : Change U9 PN to ARBL5MV0000	
			Page24 : PD XD_WPO#_C with R491(reserve) for XD measure	
			Page26 : Change the footprint of DFFC34FR003 from 88171-3400L-34P-L to 91504-340N-34P-L.	
			Page20 : Change L1, L2 and L3 to CX8LL470000. Change C1, C2, C4, C5, C6 and C8 to CH-686T0B07 for EA CRT measure pass	
			Page16 : Change R345 Value to WOHM@10K_4 and Change R548 to WOGS@10K_4	
			Page26: Apply FA@ at Felica function Parts Value	
			Page27 : Apply MAIN@ at Q26,Q27,R374 and R375	
			Page30 : R516 change to C659, R543 change to C658	
			Page31 : Apply varistor PD11 and PD12 to BCDA204UZ09 for ESD request	
			Page30 : Apply ESD8, ESD9(BC03220KZ19) and C660 in HP_JP for ESD solution.	
			Page27 : Change R374 and R375 from 390ohm to 150ohm base on ME request for LED light not enough	
			Page27 : Modify New card footprint to NCARD-13180151-U-26P-L-TE1	
			Page26 : NC CN13 pin3 to follow LED board	
			Page31 : PL6 change PN to CDRH104R-TE1	
			Page19 : Apply PN in R10 to CS33742FB17	
			Page14 : Modify RTC circuit to follow BL5S	
			Page30 : Remove 1412 Amp circuit	
			Page29 : Modify speaker gain to 9.7dB, R334 and R348 change to CS31053F909, R572 and R576 change to CS31603F916	
			Page27 : Change new card power switch to TI (AL002231000)	
			Page24 : NC C542 for customer request. O2 spec can't oevr 10p	
	E3A-01	20080125	BOM release	
			E3A-01	
			Page30 : Change C651 and C652 to 0_6	
			Page24 : Change R488 to 33_4	
			Page32 : Change PR76 to 10K/F and stuff PR77 to 64.9K/F	
			Page24 : Change VR1 PN to CK0000RZ006	
			E3B	
			Page14 : remove T50	
			Page19 : apply R14 Value to LED@	
			Page25 : remove R312, R301 and R327	
			Page21 : CN23 apply IEHM@ in Value	
			Page31 : PC25 change to CY060320901 for ESD	
			Page27 : NC C264 and R253 from CS32872FB11 change to CS00002JB38	
			F3A	
			Page? : EC Pin 27 connect to DISPON	
			Page22 : Q38 pin2 change to +3V_S5	
			Page19 : Change CN4 to DFFC04FR012	

Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	Change list	1A

Date: Wednesday, February 13, 2008 Sheet 40 of 41